(19) Europäisches Patentamt
European Patent Office
Office européen des brevets

(11) Publication number: **0 575 676 A1**

(12) EUROPEAN PATENT APPLICATION

(21) Application number: **92305930.7**

(22) Date of filing: **26.06.92**

(51) Int. Cl.5: **H03K 19/00**, H03K 19/0185, H03K 19/003

(43) Date of publication of application:
29.12.93 Bulletin 93/52

(84) Designated Contracting States:
AT BE CH DE DK ES FR GB GR IT LI LU MC NL PT SE

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(54) Logic output driver.

(57) A programmable logic output driver includes a bias generator (100), a current mirror (200) and an output stage (300), there being a digital programming feature to maintain the output voltage slew rate at an acceptable value for either high or low values of load capacitances. The driver is programmable and can maintain a constant value of driver output resistance in the circumstances where the load voltage approaches the full swing logic voltage. In the preferred embodiment, the programmed output resistance is independent of variations in process, temperature and VDD supply voltage. TTL loads are driven with the minimum amount of required output current. Because of the constant resistance, the driver supplies a specified amount of current to the load even when the load is pulled down to a specified voltage. The resistance value is substantially the highest value possible consistent with providing a required minimum load drive current and the resistive damping of the output RLC circuit is maximized so that voltage "kick" or "undershoot" is held to a minimum.

EP 0 575 676 A1

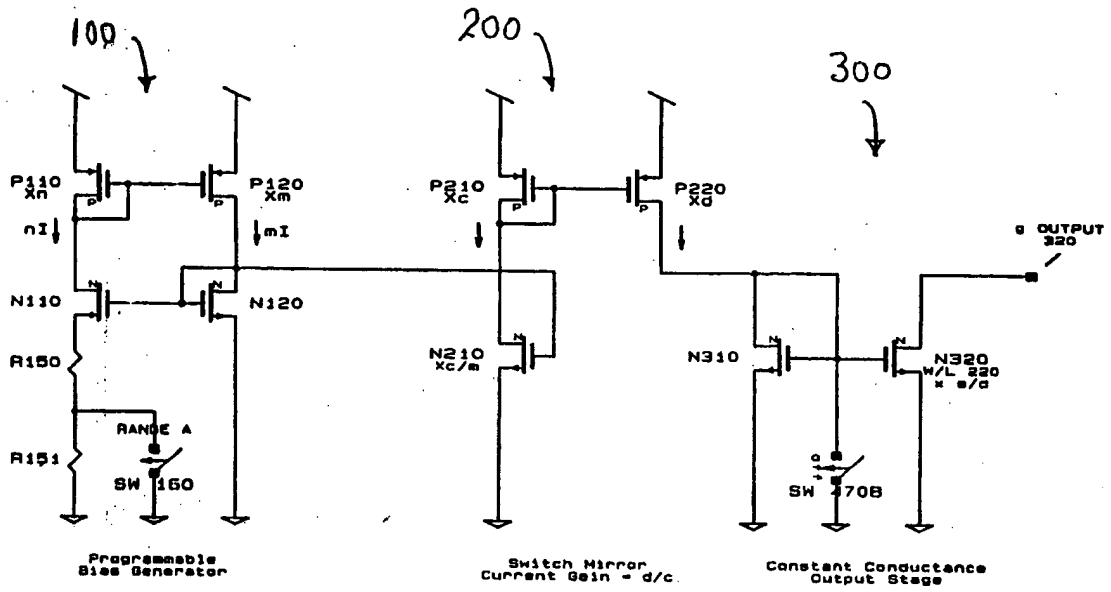

Figure 2
Programmable Conductance
Output Driver

This invention relates to CMOS logic output drive circuitry, particularly circuitry which is used to drive logic signals off chip into TTL (transistor-transistor logic) loads.

Typical prior art output circuits used to drive TTL loads employ high current CMOS output drivers. These drivers suffer from several limitations. One limitation is that the output current provided by a simple CMOS output driver depends on several process-dependent parameters such as device mobility and gate oxide thickness. Some process-dependent parameters such as mobility in turn depend highly on operating temperature.

Another weakness of simple CMOS drivers is that the output current provided depends on the input voltage, which is usually equal to the VDD power supply voltage. This VDD voltage may, however, vary by as much as +/- 10 percent. To account for all process, temperature and voltage effects, output drivers may be designed to nominally provide more output current than the minimum required to drive the load. This "safety margin" ensures that there will be enough current to drive the output load, but for a fast process, with high mobility and high drive currents, the output current provided may be several times the minimum required.

Drive currents provided by CMOS chips may even have to be increased beyond the minimum DC requirements in cases where high-capacitance loads are encountered. In the case where such a semiconductor chip drives low-capacitance loads, severe problems may then result from a high current driving a low capacitance. This causes a high voltage slew rate (rate of change of voltage per unit of time). A high voltage slew rate such as 2 volts per nanosecond may inject noise into the driver circuitry, and this may upset the data stored in some sensitive circuits such as CMOS dynamic memories.

As is well known in the art of digital design, TTL logic devices have two principle voltage states: a HIGH state, with a voltage above a given upper threshold (the output becomes a digital "1") and a LOW state, in which a voltage is below a given lower threshold (the output becomes a digital "0"). The TTL device may typically assume either state at its input and output.

It is usually preferred that the TTL device be able to switch quickly from one state to another and an output driver must therefore be able to source or sink output current quickly. An additional problem is thereby encountered in high-speed output drivers when the load voltage drive rapidly nears the full swing logic 0 voltage. As the output nears 0, the output current drive changes rapidly and a high transient voltage may be produced across the lead and track inductance in series with the load. It is well known that the voltage across an inductance increases in direct proportion to the size of the inductance and the time rate of change of current. The voltage "kick" or "undershoot" across the inductance may thus be large enough to turn on parasitic diodes in the loads and generate noise currents that upset the logic state of the load (the state of the attached load may switch inadvertently from a "1" to a "0" or vice versa) or even cause the device to fail in a mode known as "latch up."

According to one aspect, the invention provides a programmable logic output driver including a digital programming feature to maintain the output voltage slew rate at an acceptable value for either high or low values of load capacitances, the driver being operable so that it can maintain a constant value of the driver output resistance in the circumstances where the load voltage approaches the full swing logic voltage. Other aspects of the invention are exemplified by the attached claims.

In a preferred embodiment, the driver has a programmed output resistance that is independent of variations in process, temperature and VDD supply voltage. Such a driver can thus drive TTL loads with the minimum amount of required output current. Because of the constant resistance, the driver can be designed to supply a specified amount of current to a load even when the load is pulled down to a specified voltage. The resistance value is substantially the highest value possible consistent with providing a required minimum load drive current and the resistive damping of the output RLC circuit is maximized so that voltage "kicks" or "undershoot" is held to a minimum. According to this preferred embodiment, the output of a programmable bias generator is used to control the input gate of a switched current mirror, which provides a predetermined current gain. The output from the current mirror in turn controls the gate of an output drive device, but this gate can also be shunted to ground by a controllable switching device.

According to another aspect of the invention, a MOS device is included in one path to ground of the current mirror in order to compensate for the added resistance of a programmable switch included in the bias generator.

According to yet another aspect of the invention, a current generator that generates a small holding current which, under the control of a separate control signal, provides a holding current to the output drive device.

In yet another embodiment of the invention, multiple, controllable, switch mirrors and a mirror selection circuit are provided so that additional ranges for changing the conductance of the output stage are incorporated.

It will thus be apparent that aspects of this invention can be implemented to provide an output driver that is programmable in order to maintain output voltage slew rates at an acceptable value for either high or low values of load capacitances. Moreover it is possible to provide an output driver which can be set so that the driver output resistance is substantially constant in the regime where the load voltage approaches the full swing logic voltage, whilst the programmed output resistance is independent of variations in process, temperature and VDD supply voltage.

Two significant benefits are derived from achieving constant output resistance, independent of process and supply voltage. The first is that in order to drive TTL (transistor-transistor-logic) loads properly, a specified amount of current must be supplied to the load when it is pulled down to a specified voltage. By considering the well known Ohms Law ("current equals voltage divided by resistance"), it is apparent that an output with constant resistance characteristics can always provide the specified minimum current at the specified minimum voltage because the ratio of a constant voltage to a constant current is a constant resistance. The second benefit is that by providing a constant driver output resistance, the resistor-inductor-capacitor (RLC) characteristics of the load are constant in the region where the output voltage nears the full swing logic voltage, especially logic 0. Because the resistance value is substantially constant and at the highest value possible consistent with providing a required minimum load drive current, the resistive damping of the output LC circuit is maximized and voltage "undershoot" or "kicks" are held to a minimum.

For a better understanding of the invention and to show how the same may be carried into effect, reference will now be made, by way of example, to the accompanying drawings, in which:

FIG. 1 is a schematic diagram illustrating a prior art bias generator;

FIG. 2 is a schematic diagram that shows generally certain principle features of one embodiment of the invention;

FIG. 3 is an embodiment of a programmable reference generator showing additional MOS devices used to compensate for the parasitic resistance of the MOS switches used in the programming;

FIG. 4a is a simplified schematic diagram illustrating the addition of power saving features to the programmable conductance output driver;

FIG. 4b is a timing diagram showing the relationship between input data and internal control signals;

FIG. 4c illustrates a control logic structure that can implement the required relationships shown in the timing diagram of FIG. 4b;

FIG. 5 is a schematic diagram showing MOS devices used for switches in a switched current mirror;

FIG. 6(a) is a schematic of a switch mirror block;

FIG. 6(b) is a symbolic representation of the switch mirror; and

FIG. 7 illustrates an embodiment of the invention providing the programming of four output conductance ranges.

A bias current generator according to the prior art is shown in FIG. 1. The gates of two P-channel devices P110, P120 are connected, as are the gates of two N-channel devices N110, N120. The sources of P110 and P120 are connected to a source of supply voltage and their drains are connected to the drains of the corresponding N-channel devices N110 and N120, respectively. The drains and gates of both P110 and N120 are connected. The source of N120 is connected to ground as is the source of N110, albeit over a resistor R150.

Assume that the N-channel devices N110 and N120 have the same effective width-to-length ratios W_e/L_e. Assume also that the P-channel devices P110 and P120 are constructed using m and n multiples of unit devices with the same W/L ratio. In such case, the total current through device P120 will be ml, the total current through device P110 will be nl and the ratio of current in P120 to P110 will therefore be m/n. With these conditions it can be shown using well known formulae that the operating conditions for the N-channel devices are given by:

E1: $\text{Beta} \cdot W_e/L_e \cdot (V_o - V_t) = (2/R_{150}) \cdot (\text{sqrt } m/n) \cdot (\text{sqrt } m/n - 1)$

where Beta is the product of mobility and oxide capacitance, V_o is the NMOS gate voltage, V_t is the NMOS threshold, "sqrt" indicates the square root operator, and R_{150} is the value of the resistance of the resistor so labelled. Sometimes, the quantity $(V_o - V_t)$ is expressed as the effective gate drive, that is, $V_o - V_t = V_e$. Making this substitution, the expression above becomes:

E2: $\text{Beta } W_e/L_e \ (V_e) = (2/R_{150}) \ (\text{sqrt } m/n) \ (\text{sqrt } m/n - 1)$

This kind of bias circuit is commonly used in the prior art to establish a bias reference voltage for a constant current generator. The bias voltage V_e can then be found simply by re-arranging the terms in the last equation to yield:

E3: $V_e = [(2/R) \cdot (\text{sqrt } m/n) \cdot (\text{sqrt } m/n - 1)] \ / \ [\text{Beta} \cdot W_e/L_e]$

Unfortunately, the effective gate drive V_e is not constant over process or temperature in the bias generators of the prior art. Neither is the drain current constant, because the drain current Id for a MOS device in saturation is given by the known formula:

E4: $Id = Beta\ (W_e/L_e)\ (V_e)^2$

The embodiment of FIG. 2 improves upon the prior art generator shown in FIG. 1 by providing a programmable output conductance for a switchable output driver N320. As FIG. 2 shows, a modified bias generator is connected to a switched current mirror, which in turn is connected to a constant conductance output stage.

As FIG. 2 shows, the drain of N120 in the bias generator is connected to the gate of an N-channel device N210, whose source is grounded. A switch SW 160 and a resistor R151 are, furthermore, added in parallel to the bias generator between the resistor R150 and ground.

Supply voltage is connected to the sources of devices P210 and P220, which form either side of a conventional current mirror. The drain of P210, however, is connected to the drain of the N-channel device N210, which controls the voltage at the gates of current mirror devices P210 and P220, as well as at the drain of P210. As is common in current mirrors, the gate and drain of the device P210 are connected to the gate of the following P-channel device P220, whose source is connected to the supply voltage and whose drain is connected as described below to a constant conductance output stage.

The operation and implementation of current mirrors are well understood by designers of digital integrated circuits and are therefore not described in further detail here. Of note, however, is that the current of device P210 is cI, while the current of device P220 is dI. The increase, or gain, in current is therefore equal to dI/cI = d/c.

As FIG. 2 shows, the source of P220 is connected to a constant conductance output stage, more particularly to the gate and drain of an N-channel device N310, to the gate of an N-channel output drive device N320 and to ground via a switch SW470B. The gate and drain of N310 are connected, and the source of N310 is grounded. The gates of N310 and N320 are connected.

The drain of the output drive device N320 is connected to the output line of the circuit, which will normally be tied to the TTL device the system is to drive. The source of N320 is grounded.

Because the programmable bias generator is coupled to the output driver through a current mirror, with current gain that is independent of process, temperature and voltage, the output driver N320 provides a programmable drive logic signal that has several desirable properties that are also independent of process, temperature, and voltage.

The independence of the output conductance of the output driver N320 from process, temperature and voltage may be seen from the commonly used equation for output conductance $g_{o[320]}$:

E5: $g_{o[320]} = Beta \cdot (W_e[320]/L_e[320]) \cdot (V_e[320])$

Note that if the devices N310 and N210 are made equal in size, the effective gate drive of N310 and output device N320 may be increased in accordance with the current gain d/c of the switched mirror. The mirror current gain is fixed at d/c since the P-channel devices P210 and P220 are preferably constructed using c and d multiples of unit devices with the same width-to-length ratio W/L.

Using known formulae one can show that the effective gate drive $V_{e[320]}$ of N320 is related to the effective gate drive V_e of the programmable bias generator simply by the square root of the mirror current gain d/c, thus:

E6: $V_{e[320]} = V_e\ sqrt(d/c)$

A combination of expressions E2 and E4-E6 above then yields the following:

E7: $g_{o[320]} = sqrt(d/c) \cdot [2/(R_{150})] \cdot (sqrt\ m/n) \cdot (sqrt\ m/n-1)$

In the bias generator, switch SW 160 provides a resistance value of R150 between the source of N110 and ground when it is closed, since resistor R151 will be shunted. When switch SW 160 is opened, however, the resistance value will be $R_{150} + R_{151}$ (since source current will then have to pass through both resistors) and the driver output conductance will be decreased, as can be seen from the following expression, in which the denominator of the second term in the right-hand side is increased from R_{150} to $(R_{150} + R_{151})$:

E8: $g_{o[320]} = sqrt(d/c) \cdot [2/(R_{150} + R_{151})] \cdot (sqrt\ m/n) \cdot (sqrt\ m/n-1)$

As is mentioned above, this decrease is desirable when driving low-capacitance loads.

Switch SW 470B is used to turn on the output current when it is in the open condition as shown. For a positive logic output, the open condition would correspond to a logic "0", or a LOW voltage output. For a logic "1" output, SW 470B would be closed, whereby the gate voltage on N320 would drop to a value sufficiently low to turn N320 off.

The delay time to turn on the output drive device N320 tends to be constant since the current driving the gate of N320 tends to track the same variations in process, voltage, and temperature as does the variation of V_e. For example, as V_e increases with temperature to require that a higher turn-on voltage be reached, the input current to the output device will increase in the same proportion because it is derived from a constant conductance generator.

Noting now that $Beta \cdot (W_e/L_e) \cdot V_e^2$ may be rewritten as $V_e \cdot [Beta \cdot (W_e/L_e) \cdot V_e]$, one may then combine expressions E4 and E5 (taking the general version of E5 rather than the specific equation for $g_{o[320]}$) to yield:

E9: $I = V_e \cdot G$

The delay time T required for the input voltage to traverse the span V_e is therefore:

E10: $T = V_e \cdot (C_{input}/I) = C/G$

Where the input capacitance is determined largely by the gate capacitance of the output device, which typically varies less than 5 percent, the variation in T will therefore be small since G is independent of process and temperature.

The programming switch SW 160 shown in FIG. 2 may alternatively be provided with a bond wire jumper, or preferably a MOS switch. Such an arrangement is shown in FIG. 3. With reference to FIG. 3, as the bias generator is provided with a MOS switch, then a MOS device such as N160 is added to the generator to compensate for the added resistance of either switch N170 or N180. Where N170 or N180 are equal in size, and the ratio of current between the devices P110 and P120 is m/n (as is indicated in FIG. 3), the appropriate sizing for N160 is just sqrt(m/n) times the size of switch N170 or N180. This sizing assures the same voltage drop across N160 as across N170 or N180.

Also with reference to FIG. 3, where the bias generator drives the input stage of a current mirror which produces an output current cI, then an additional device N280, with a width-to-length ratio W/L of c/sqrt(mn) is added to the mirror to compensate for the switch effects. This W/L value assures that the voltage drop across N280 will be equal to the voltage drop across N160.

The advantage provided by the compensating MOS devices N170, N180 and N280 of FIG. 3 is that they greatly reduce the temperature-dependent and process-dependent effects of the switches N170 and N180 in causing variations in the programmed value of output conductance. The primary variations in output conductance will then depend only on the temperature coefficient and accuracies of resistors chosen for R150 and R160. These resistors may be polysilicon resistors, well resistors, or deposited film resistors, depending on available processes, specific resistance value, and the required temperature coefficient.

FIGS. 4a-4c illustrate two improvements to the embodiment of the invention shown in FIG. 2. Both improvements result in reduced standby power for the output driver.

The switched current mirror of FIG. 2 passes current continuously, even when the circuit is not required to provide an output current as is the case when S470B is closed. The improvement in FIG. 4a is the addition of switches SW260A and 260B, which interrupt the flow of current from device N210 to P220 and short out the gate of P210 to the positive supply voltage. Both of these actions cause the current flow cI and dI to be reduced to zero after the high-current initial phase of driving a capacitive load is no longer required.

Once the current from P220 has been forced to zero, some minimum value of output current drive must be provided by output device N320. This minimum value of output current is provided by a small holding current generator (labelled "i gen" in FIG. 4a), which passes current hI through switch SW 470A and across device N420. Even this small holding current hI is not required for a data output of logic "1" when SW 470B is closed and no current flows through output device N320. Consequently, the holding switch SW 470A is closed when the "N ON" is HIGH, whereas the switch SW 470B at the gates of N310 and N320 is in the open position for the "N ON" portion of the timing cycle.

A load capacitance charging signal CHG controls the state of a switch between the supply voltage and the gates of the devices P210 and P220 in the current mirror. This charging signal CHG need be present for only as long as required to assure that the load capacitance has rapidly reached the full logic output voltage. The CHG signal may be generated for the required amount of time by any conventional logic circuitry that detects transition of input data from the logic "0" to the logic "1" value.

FIG. 4b illustrates the timing relationship between the signals N ON, its inverse N OFF, the charge signal CHG and the state of an input data bit DATA IN. An example of suitable detection circuitry that has these timing characteristics is illustrated in FIG. 4c, but other circuits may also be used together with the invention. Theory and experience indicate that the CHG signal will be required for less than 100 nanoseconds in typical applications.

The signals CHG, N ON and N OFF may be generated in a circuit indicated generally as circuit

600 in FIG. 4c. Referring to this figure, when the input data (DATA IN signal) transitions from a "1" to a "0" as shown in FIG. 4a, an MOS capacitor N620 will no longer be clamped to ground, but rather will begin to charge through a switch P630. The switch P630 receives a constant current from the constant current generator consisting of the 16k resistor (for example) and the mirror P610, P620.

Immediately when the DATA IN signal changes from a "1" to a "0", N ON changes from a "0" to a "1" and the convention NAND gate output changes from a "1" to a "0". The output from the NAND gate passes through an inverter an becomes the CHG signal, which changes from a "0" to a "1". This CHG signal is then routed to the switch mirror, whereas the N ON signal is used to turn on the small holding current generator.

As the MOS capacitor N620 charges past the logic threshold of the inverter connected to its top plate, (its gate), the inverter output changes from "1" to "0" and causes the NAND gate output to rise from "0" to "1", thereby driving the CHG signal from "1" to "0". The size of the MOS capacitor may be chosen for any desired duration of the CHG signal, for example, from 10 to 100 nanoseconds.

When the DATA IN signal changes from "0" to "1", the CHG signal is immediately terminated and the MOS capacitor discharges rapidly through the N-channel device N610. At the same time, the N ON signal changes from "1" to "0" and immediately turns off the small holding current generator. The N OFF signal (the inverse of N ON) also changes from "0" to "1", turns on the switch SW 470A, and immediately turns off the output driver N320 by shorting its gate to ground. The switch and charging control signals N ON, N OFF, CHG, and those applied to the various switches in the embodiments of the invention may alternatively be generated in a known manner by other conventional hardware structures.

FIG. 5 is a schematic diagram showing the MOS devices preferably used to implement the various switches in the system that are controlled by the CHG signal. Thus, the P-channel MOS device P260B corresponds to the switch SW 260B in FIG. 4a; switch SW 260A is implemented by P260A; and switch SW 360 is implemented by the N-channel device N360. Also, switch SW 470 B, which is controlled by the N OFF signal, is shown implemented by the N-channel device N470B. The implementation of simple switches such as these is well understood in the field of circuit design.

In FIG. 6a and 6b, the switched mirror and its symbolic block representation are shown. In this block representation, the switched mirror receives the input signal INPUT as before from the drain of the device N120 of the bias generator (see FIG. 5). An ON signal is also applied to the mirror; this ON signal corresponds to the CHG signal shown and described above. As FIG. 6b indicates, the current mirror acts to provide an output current that is d/c times its input current; this is also described above.

A switched current mirror using a lower current ratio than the ones used for the charging current may be used to provide the small holding current generator indicated in FIG. 5. Such an arrangement is shown in FIG. 7.

In the embodiments described above, a single switched current mirror stage with a current gain of d/c is included between the bias generator and the constant capacitance output stage. The system according to the invention is not limited to such single-value implementations.

FIG. 7 illustrates an embodiment of the invention which provides four charging current ranges for programming. Two switched mirrors are included to provide two programmable levels of output current from the generator at output devices N320A or N320B. The two switched mirrors preferably have the same structure as described above for the single-mirror implementations and are indicated generally at 510 and 550 in FIG. 7.

Note that the output stage in this embodiment includes a pair of output devices N320A and N320B, each corresponding to the single driver N320 in FIG. 5, as well as a set of gate control devices corresponding to N310, N360 and each with a switch N370A, N370B corresponding to the single switch N470B in FIG. 5. The drains of the two output drive devices N320A and N320B are connected. The gates of the devices N360A and N360B are connected to the CHG signal. The drains and gates of devices N310A and N310B are connected, respectively, to the outputs of the switch mirrors 510 and 550 (controlled by the CHG signal) and 410 and 450 (controlled by the N ON signal. These current mirrors preferably have the structure shown in FIGS. 6a and 6b.

According to this embodiment, switch mirror 550 is enabled only if the "RANGE C" programming control circuit is a logic "0". In that case, a P-channel device P660 in a RANGE C Switch 700 (which forms a mirror selection switching device) is driven into a conductive state and the bias generator output voltage at the drain of N120 is allowed to pass to the input of switch mirror 550.

In the case that the switch mirror located at 550 is to be disabled by a logic "1" for the RANGE C control signal, P660 is cut off and N660 is turned on and grounds the input of switch mirror 550. In addition, device N670 is turned on to return any leakage current from mirror 550 output to ground and to assure that the output driver N320B is turned off.

Holding current mirrors 410 and 450 provide a small holding current to guarantee that the N320A and N320B outputs remain on at a desired output conductance value after the initial charging phase is complete. By using switch mirror blocks as shown in FIGS. 6a and 6b, which are connected to the input bias generator, the driver output conductance level is constant and independent of process, temperature and power supply variation.

Holding current mirrors 410 and 450 must be turned off to save power when the data input is a logic "1". This is accomplished by using the signal N ON to drive an ON input to each switch mirror 410, 450. The N ON signal is derived from an inverter connected to the logic input, and is thus the logical inverse of the input data bit. Switch devices N370A and N370B short all switch mirror leakage current to ground in response to the N OFF signal (the logical inverse of N ON) when the data input is a logic "1". These switches assure that output devices N320A and N320B are turned off. The N OFF signal is derived from a logic buffer consisting of two inverters connected is series and to the data input (see FIG. 4c).

By varying device sizes and current gains in the switched mirrors 510 and 550 and also by varying the sizes of the output devices N320A and N320B, many possible programming ranges may be provided. The highest output conductance in the preferred embodiment is programmed by setting RANGE A (at the input of the bias generator) equal to logic "1" and RANGE C equal to a logic "0". Although four programming ranges may be selected by the combination of the RANGE A and RANGE C logic signals in the embodiment of FIG. 7a, many more programming ranges are possible by using additional programming resistors or switched mirrors. In other words, more than two complete switch mirrors 510/410 and 550/450 may be included, as long as additional selection switches are included in the RANGE C switching device and suitable control signals are provided as above.

Additionally, the invention is not restricted by the polarity of the embodiments illustrated in the figures. The invention may be easily extended using known methods to add switched mirrors and output drivers of opposite polarity to drive CMOS loads, or use alternate semiconductor technology to drive loads of different output voltages or signal polarities.

Claims

1. A logic output driver, for driving an attached logic device, including a bias generator (100) and an output stage (300),

   CHARACTERIZED in that:

   a current mirror (200; P210, P220) is connected to the bias generator (100), the output stage (400) is connected to the current mirror (200) and at least one of the group consisting of the bias generator (100), the output stage (300) and the current mirror(200) is programmable, the driver being such that the conductance of the output stage (300) can be held substantially constant at a selected one of a predetermined number of predetermined conductance values substantially independent of changes in process, supply voltage and temperature.

2. A logic output driver according to claim 1 wherein the bias generator (100) is programmable.

3. A logic output driver according to claim 1 or 2, wherein the current mirror (200) is programmable.

4. A logic output driver according to claim 1, 2 or 3, wherein the output stage (300) is programmable so that its conductance can be changed.

5. A logic output driver according to any one of the preceding claims wherein the bias generator is a bias current generator (100) including a bias current mirror (P110, P120) and a pair of bias output devices (N110, N120).

6. A logic output driver according to claim 5, wherein the current mirror is a switchable current mirror (P210, P220) with a switchable mirror input gate (N210) connected to a bias current output of the current generator.

7. A logic output driver according to claim 6, wherein a pair of bias resistors (R150, R151) is included in the path to ground of a predetermined one of a pair of bias output devices of the bias generator and a pair of bias programming switching devices (N170, N180) is included in the path to ground of the same bias output device as the bias resistors (R150, R151), a resistance compensation device (N160) being included in the switchable current mirror to compensate for the resistance of the bias programming switching devices (N170, N180).

8. A logic output driver according to any one of the preceding claims wherein the output stage (300) includes an output drive device (N320) and there is a two-state output semiconductor switch (SW 470B) to conduct and shunt a gate of the output drive device (N320) when an

input data bit has a first state and to open when the input data bit has a second state.

9. A logic output driver according to any one of the preceding claims and comprising a switchable current holding circuit, comprising a holding current generator (i_gen) and a holding switch (Sw 470A), included in the output stage to maintain a minimum output current at a predetermined slew rate into the load when the load is in a low logical state.

10. A logic output driver according to any one of the preceding claims, wherein the current mirror includes a quick-charging arrangement (600) that generates a charging signal (CHG) as a predetermined function of state transitions of the load.

11. A logic output driver according to any one of the preceding claims and including a switchable mirror array including a plurality of switch mirrors (510, 410; 55, 450), each having a different output current, and a mirror selection device (700) connected to the switch mirrors that activates a selected one of the switch mirrors depending on the state of a selection input signal (RANGE_C).

12. An output driver for providing a signal to a load, including,

a bias generator for providing a control current,

first means responsive to the control current from the bias generator for providing a particular gain in the output current, such gain being independent of variations in process, temperature and voltage,

second means responsive to the particular gain in the output current from the first means for providing a constant conductance,

third means for providing a binary logic signal having first and second logic levels, and

fourth means operatively coupled to the second means and responsive to the binary logic signal for providing for the substantially constant conductance in the third means in accordance with the first binary logic level in such binary logic signal and for preventing the operation of the second means in providing the substantially constant conductance in accordance with the second binary logic level in the binary logic signal.

13. An output driver as set forth in claim 12, including,

the load being responsive to the signals from the fourth means,

fifth means included in the bias generator for providing for a decrease of the constant conductance in the fourth means for a low capacitance in the load and for providing for an increase of the constant conductance in the fourth means for a high capacitance in the load.

14. A programmable output driver as set forth in claim 12, including,

fifth means included in the bias generator for reducing temperature-dependent and process-dependent effects in the bias generator, thereby reducing any variations in the substantially constant conductance in the fourth means from temperature-dependent and process-dependent effects.

15. An output driver as set forth in claim 12, including,

fifth means included in the first means for minimizing the power in the second means when the first means is in a standby state, and

sixth means included in the second means for providing a holding current in the second means when the fifth means minimizes the power in the first means.

16. An output driver as set forth in any one of claims 12 to 15, including,

the load having a capacitance, and

means included in the bias generator and the first means for expediting the charging of the capacitance in the load when the binary logic signal changes from the second logic level to the first logic level.

17. An output driver as set forth in any one of claims 12 to 16, including,

means included in the second means for providing controlled adjustments in the value of the particular gain in the output current from the first means.

18. An output driver as set forth in claim 17, including,

means included in the first means for maintaining the fourth means at the constant conductances after the capacitances in the load have been charged.

19. An output driver for providing a signal to a load, including,

a bias generator for providing a control current,

a current mirror responsive to the control current for producing in the control current a gain that is independent of variations in pro-

cess, temperature and voltage,

an output generator responsive to the gain in the control current for providing a signal to the load with a substantially constant conductance, and

first means operatively coupled to the output generator for providing an input signal having first and second logic levels and for providing for the production of the substantially constant conductance in the output generator only for the first logic level in the input signal.

20. An output driver as set forth in claim 19, including,

the load having a capacitance,

second means included in the bias generator for adjusting the value of the substantially constant conductance in the output generator in accordance with the variations in the capacitance in the load, and

third means included in the bias generator for compensating for the operation of the second means in adjusting the value of the substantially constant conductance in the output generator.

21. An output driver as set forth in claim 20, including,

the second means providing for a variable impedance in accordance with variations in the capacitance of the load, and

the third means compensating for the variations in the impedance in the second means.

22. An output driver as set forth in claim 19, 20 or 21, including,

means included in the bias generator for reducing the effects of the variations in temperature and process in the bias generator on the substantially constant conductance in the output generator, and

means included in the current mirror for reducing the effects of the variations in temperature and process in the current mirror on the substantially constant conductance in the output generator.

23. An output driver as set forth in any one of claims 19 to 22 and including,

means included in the current mirror for interrupting the flow of current through the current mirror when the output generator is in a standby operation, and

means included in the output generator for maintaining a holding current in the output generator when the output generator is in the standby operation.

24. An output driver as set forth in any one of claims 19 to 23 and including,

the output generator providing an output current, and

third means included in the current mirror and programmable to provide for different magnitudes of the output current from the output generator.

25. An output driver as set forth in claim 24, including,

a plurality of transistors in the output generator,

the sizes of the transistors in the output generator being adjustable in accordance with the programming in the current mirror to provide for different magnitudes of the current from the current mirror.

26. An output driver for providing a signal to a load having a variable capacitance, including,

means for providing an input signal having first and second logic levels,

a bias generator for providing a control current,

means included in the bias generator for providing impedances having adjustable values,

means included in the bias generator for programming the impedances to provide adjustable values in accordance with the variations in the capacitance in the load,

a current mirror for providing a gain in the control current, and

an output generator operatively coupled to the current mirror and responsive to the control current from the current mirror and to the input signal for providing a substantially constant conductance to produce the signal to the load in accordance with the first logic level in the input signal.

27. An output driver as set forth in claim 26, including,

means included in the bias generator for reducing the effects of variations in temperature and process on the production of the constant conductance in the output generator.

28. An output driver as set forth in claim 26 or 27, including,

means included in the current mirror for interrupting the flow of current through the current mirror when the output generator is in a standby condition, and

means included in the current generator for maintaining a holding current in the output generator when the output generator is in the

standby condition.

29. An output driver is as set forth in claim 26, 27 or 28, including,

programmable means included in the current mirror for adjusting the gain provided by the current mirror in the control current, and

means included in the output generator for adjusting the value of the substantially constant conductance in the output generator in accordance with the adjustment in the gain in the control current by the programmable means in the current mirror.

30. An output driver as set forth in claim 27, including,

programmable means included in the current mirror for adjusting the gain provided by the current mirror in the control current, and

means included in the output generator for adjusting the value of the substantially constant conductance in the output generator in accordance with the adjustment by the programmable means in the gain in the current mirror, and

means included in the output generator for eliminating the holding current in the output generator when the output generator produces the signal to the load in accordance with the first logic level in the input signal.

31. An output driver for providing a signal to a load having a variable capacitance, including,

a bias generator for providing a control signal,

means for providing an input signal having first and second logic levels,

a current mirror for providing a gain in the control signal,

programmable means included in the current mirror for provided a controlled adjustment in the gain in the current mirror,

an output generator responsive to the control current from the current mirror for providing a substantially constant conductance in the output generator during the production of the first logic level in the input signal and for producing an output signal for introduction to the load during the production the first logic level in the input signal, and

means included in the output generator for adjusting the value of the substantially constant conductance in the output register in accordance with the adjustment in the gain of the control current in the current mirror.

32. An output driver as set forth in claim 31, including,

means included in the current mirror for interrupting the control current in the current mirror when the output generator is operating in a standby condition, and

means included in the output generator for producing a holding current when the output generator is operating in the standby condition.

33. An output generator as set forth in claim 31 or 32, means being included in the current mirror for minimizing any effects of variations in temperature and process in maintaining the production of the substantially constant conductance in the output generator.

34. In a combination as set forth in claim 33, means for providing an adjustable impedance, and

programmable means included in the bias generator for adjusting the impedance in accordance with the variations in the capacitance in the load.

35. An output driver according to any one of the preceding claims in combination with a logic device that constitutes a load and has a plurality of states and a load capacitance.

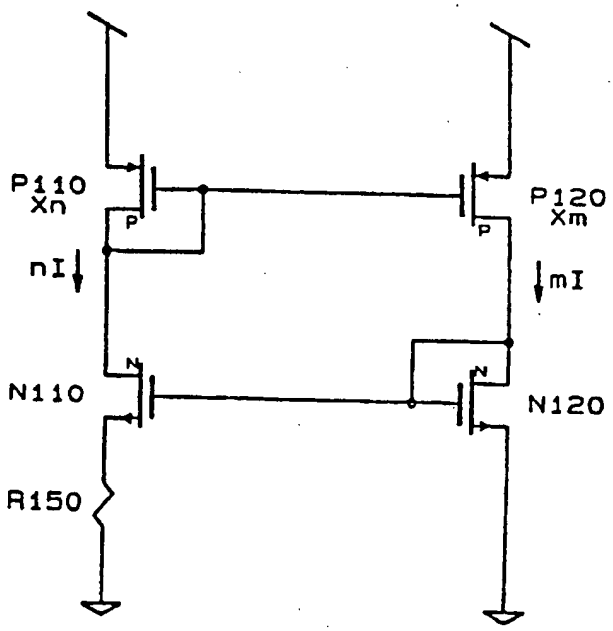

Figure 1
Bias Generator
(Prior Art)

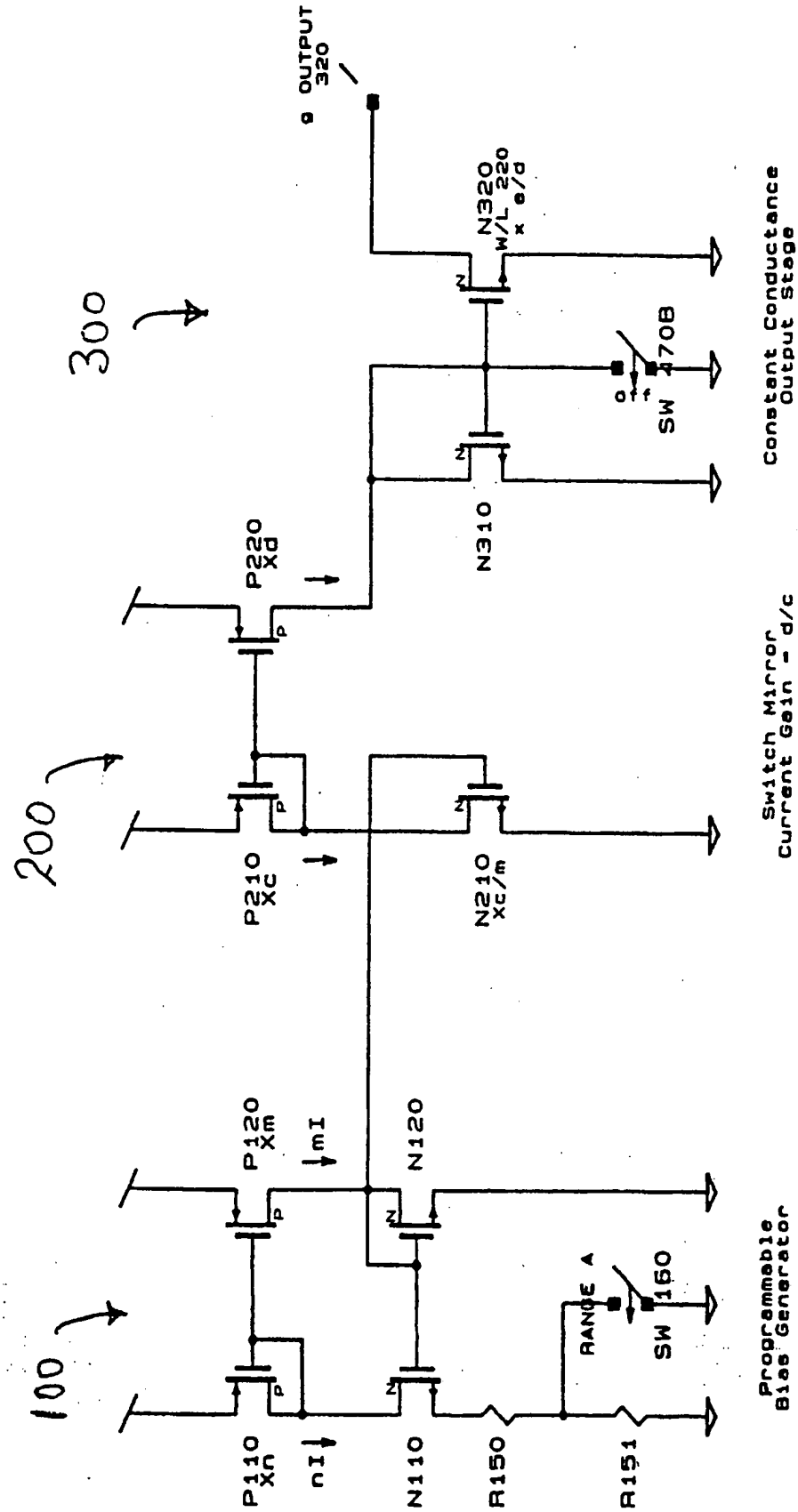

Figure 2
Programmable Conductance
Output Driver

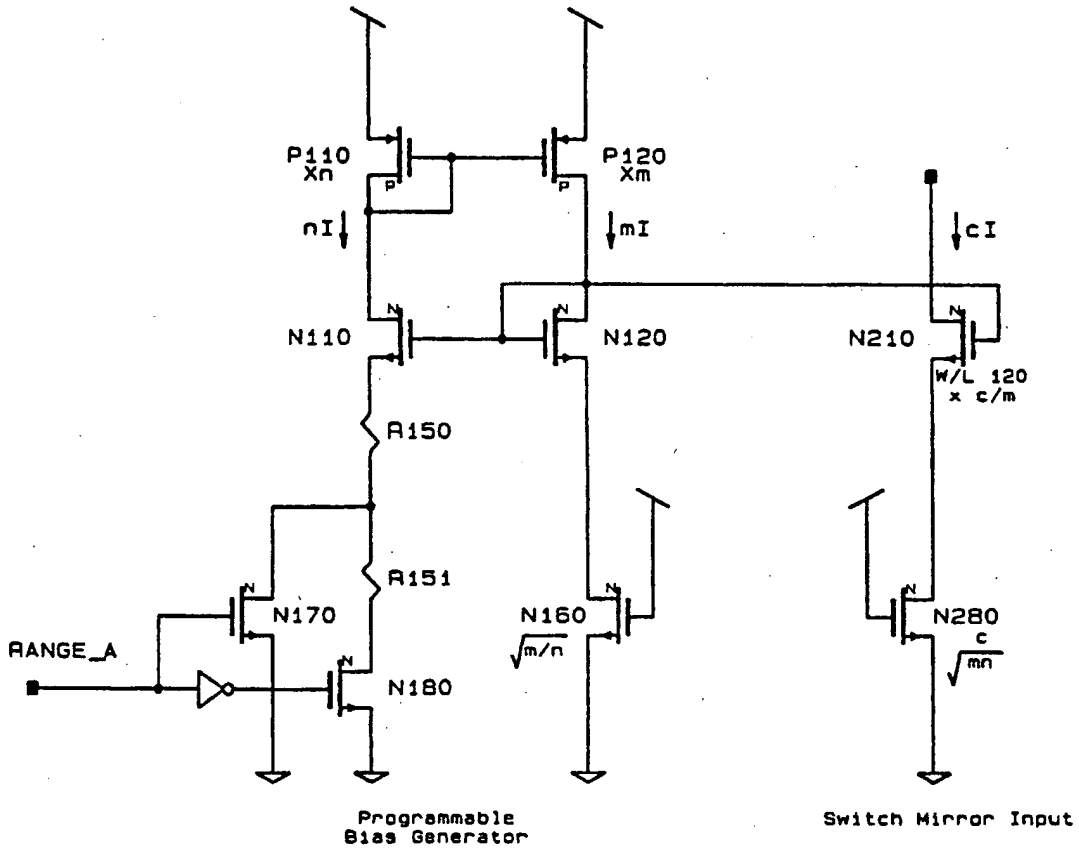

Figure 3
Programmable Reference Generator
With MOS Switching

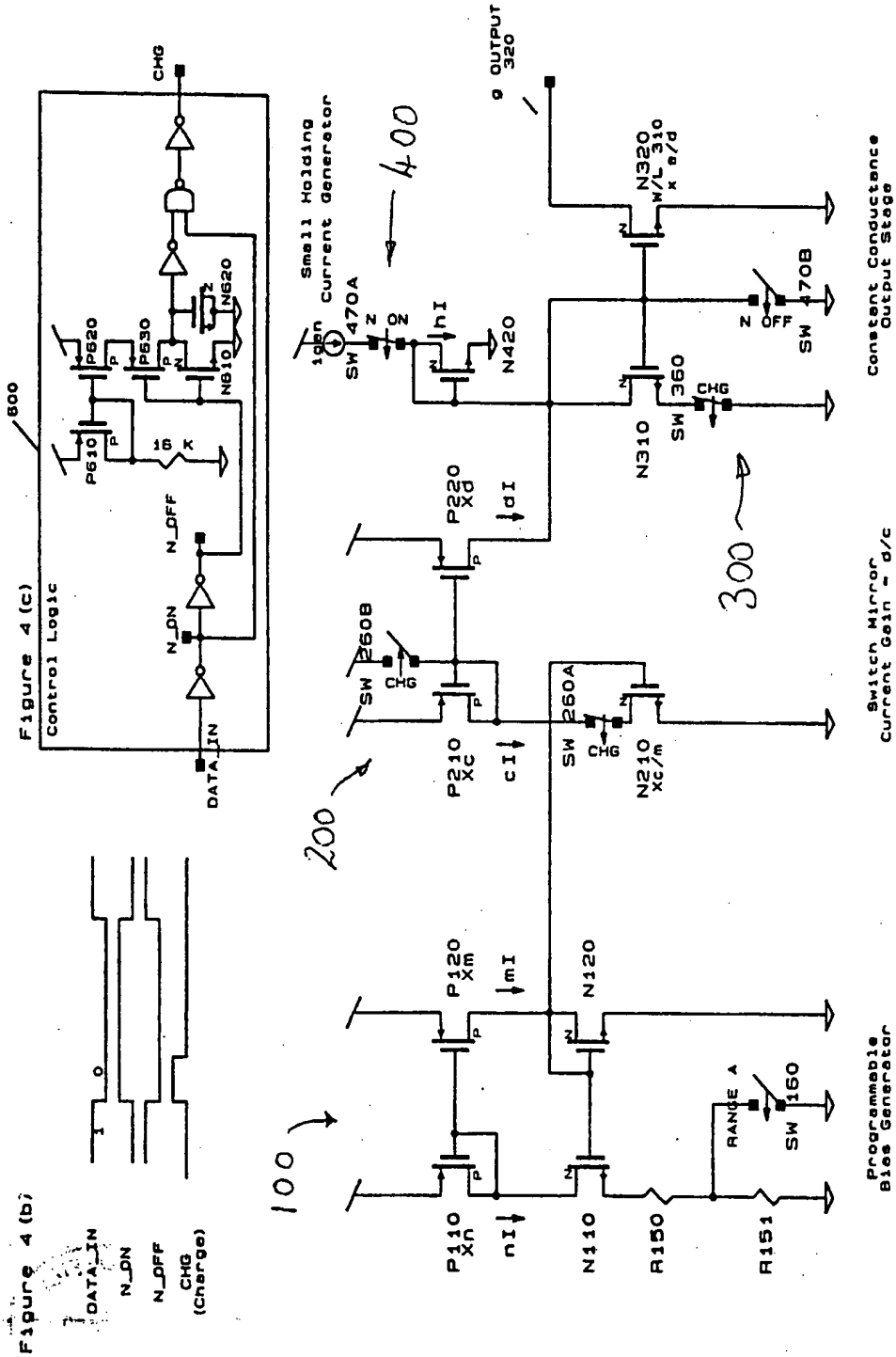

Figure 4(a)
Programmable Conductance Output Driver

Figure 4(b)

Figure 4(c)

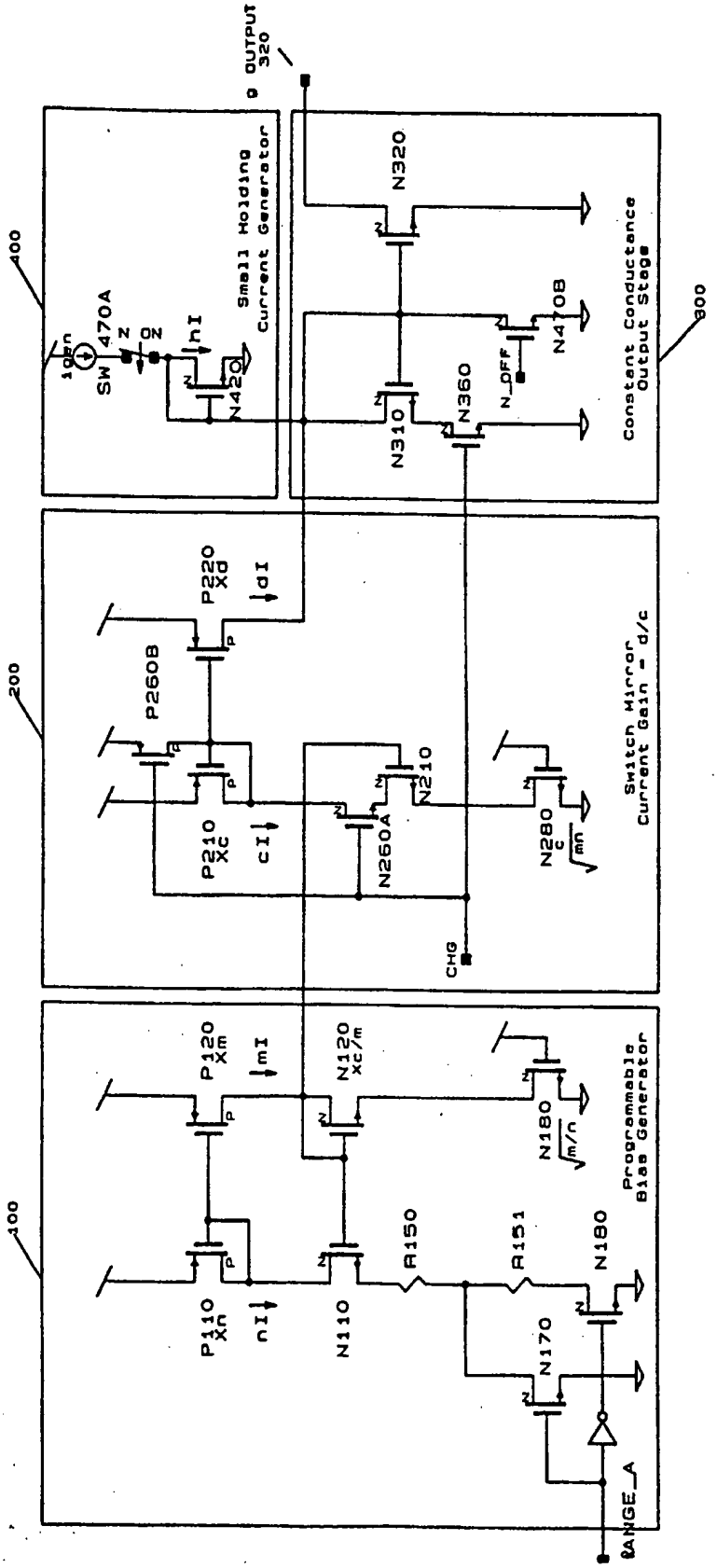

Figure 5
Programmable Conductance
Output Driver
With MOS Transistor Switching

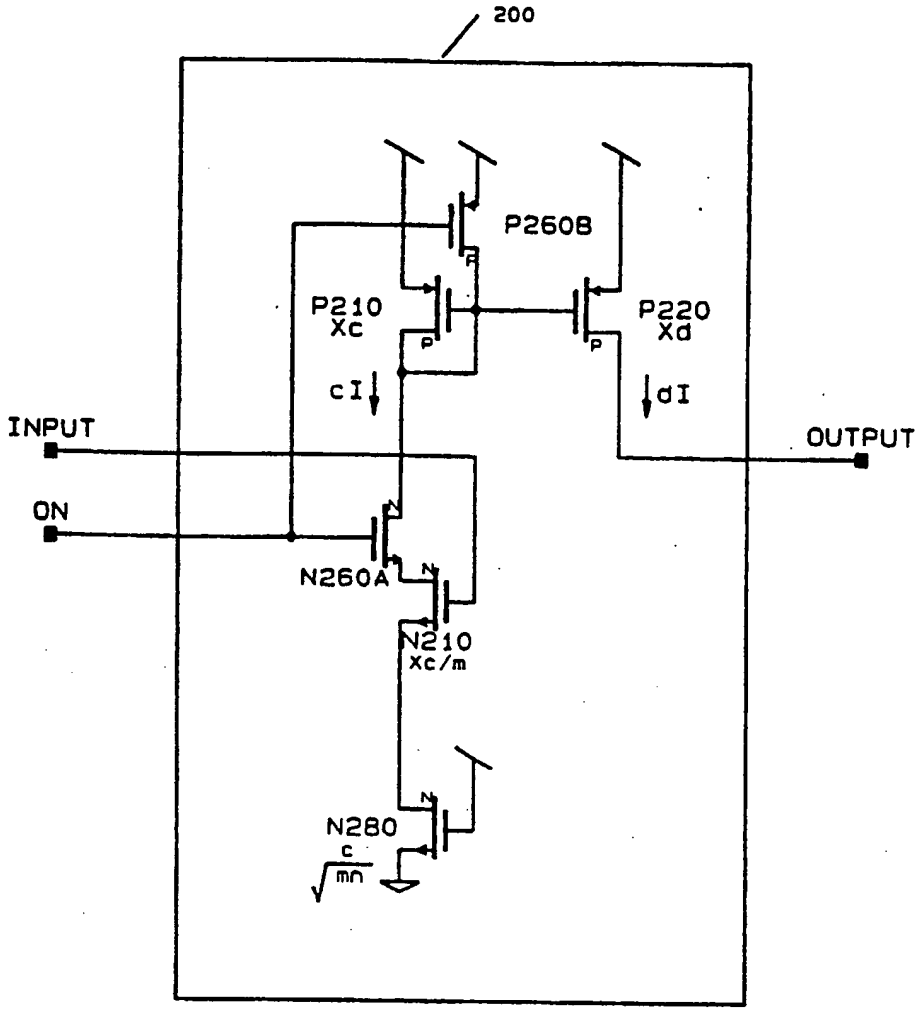

Figure 6(a)
Switch Mirror
Current Gain = d/c

Figure 6(b)
Switch Mirror
Block Symbol
Current Gain = d/c

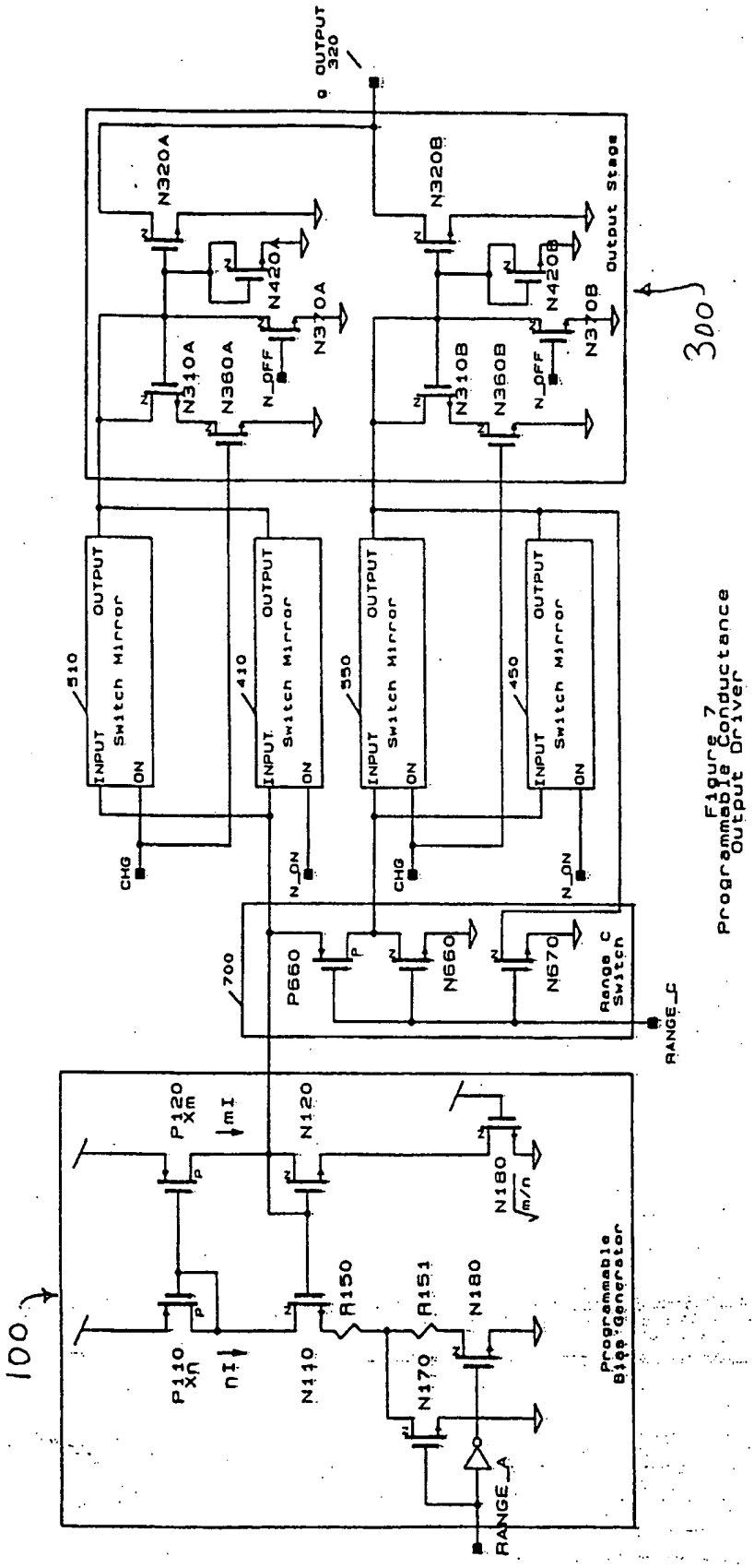
Programmable Conductance Output Driver
Output Stage
300
100
OUTPUT 320
N320A
N320B
N420A
N420B
N370A
N370B
N310A
N360A
N310B
N360B
N_OFF
OUTPUT
INPUT
Switch Mirror
ON
510
410
550
450
CHG
N_ON
700
P660
N660
N670
Range C Switch
RANGE_C
P120
Xm
mI
N120
N180
m/n
R150
R151
N180
P110
Xn
nI
N110
N170
Programmable Bias Generator
RANGE_A

Figure 7

European Patent Office

EUROPEAN SEARCH REPORT

Application Number

EP 92 30 5930

DOCUMENTS CONSIDERED TO BE RELEVANT

Category	Citation of document with indication, where appropriate, of relevant passages	Relevant to claim	CLASSIFICATION OF THE APPLICATION (Int. Cl.5)
A	US-A-4 623 799 (NYMAN,JR) ---		H03K19/00 H03K19/0185 H03K19/003
A	US-A-3 980 898 (PRIEL) ---		
A	EP-A-0 451 365 (SIEMENS) ---		
A	IBM TECHNICAL DISCLOSURE BULLETIN. vol. 30, no. 8, January 1988, NEW YORK US pages 455 - 456 'soft turn-on circuit' -----		

TECHNICAL FIELDS SEARCHED (Int. Cl.5)

H03K

The present search report has been drawn up for all claims

Place of search	Date of completion of the search	Examiner
THE HAGUE	29 JANUARY 1993	FEUER F.S.

CATEGORY OF CITED DOCUMENTS

X : particularly relevant if taken alone
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EPO FORM 1503 03.82 (P0401)

(19) Europäisches Patentamt
European Patent Office
Office européen des brevets

(11) EP 0 575 676 B1

(12) **EUROPEAN PATENT SPECIFICATION**

(45) Date of publication and mention of the grant of the patent:
29.12.1997 Bulletin 1997/52

(51) Int Cl.[6]: **H03K 19/00**, H03K 19/0185, H03K 19/003

(21) Application number: **92305930.7**

(22) Date of filing: **26.06.1992**

(54) **Logic output driver**

Logikausgangstreiber

Circuit d'attaque logique de sortie

(84) Designated Contracting States:
DE FR GB NL

(43) Date of publication of application:
29.12.1993 Bulletin 1993/52

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(56) References cited:
EP-A- 0 275 941
EP-A- 0 451 365
US-A- 3 980 898
US-A- 4 623 799

- **IBM TECHNICAL DISCLOSURE BULLETIN. vol. 30, no. 8, January 1988, NEW YORK US pages 455 - 456 'soft turn-on circuit'**

EP 0 575 676 B1

Printed by Jouve, 75001 PARIS (FR)

Description

This invention relates to CMOS logic output drive circuitry, particularly circuitry which is used to drive logic signals off chip into TTL (transistor-transistor logic) loads.

Typical prior art output circuits used to drive TTL loads employ high current CMOS output drivers. These drivers suffer from several limitations. One limitation is that the output current provided by a simple CMOS output driver depends on several process-dependent parameters such as device mobility and gate oxide thickness. Some process-dependent parameters such as mobility in turn depend highly on operating temperature.

Another weakness of simple CMOS drivers is that the output current provided depends on the input voltage, which is usually equal to the VDD power supply voltage. This VDD voltage may, however, vary by as much as +/- 10 percent. To account for all process, temperature and voltage effects, output drivers may be designed to nominally provide more output current than the minimum required to drive the load. This "safety margin" ensures that there will be enough current to drive the output load, but for a fast process, with high mobility and high drive currents, the output current provided may be several times the minimum required.

Drive currents provided by CMOS chips may even have to be increased beyond the minimum DC requirements in cases where high-capacitance loads are encountered. In the case where such a semiconductor chip drives low-capacitance loads, severe problems may then result from a high current driving a low capacitance. This causes a high voltage slew rate (rate of change of voltage per unit of time). A high voltage slew rate such as 2 volts per nanosecond may inject noise into the driver circuitry, and this may upset the data stored in some sensitive circuits such as CMOS dynamic memories.

As is well known in the art of digital design, TTL logic devices have two principle voltage states: a HIGH state, with a voltage above a given upper threshold (the output becomes a digital "1") and a LOW state, in which a voltage is below a given lower threshold (the output becomes a digital "0"). The TTL device may typically assume either state at its input and output.

It is usually preferred that the TTL device be able to switch quickly from one state to another and an output driver must therefore be able to source or sink output current quickly. An additional problem is thereby encountered in high-speed output drivers when the load voltage drive rapidly nears the full swing logic 0 voltage. As the output nears 0, the output current drive changes rapidly and a high transient voltage may be produced across the lead and track inductance in series with the load. It is well known that the voltage across an inductance increases in direct proportion to the size of the inductance and the time rate of change of current. The voltage "kick" or "undershoot" across the inductance may thus be large enough to turn on parasitic diodes in the loads and generate noise currents that upset the logic state of the load (the state of the attached load may switch inadvertently from a "1" to a "O" or vice versa) or even cause the device to fail in a mode known as "latch up."

US 4,841,175 relates to an ECL-compatible input/output circuit capable of operating independently of temperature and field effect transistor parameter fluctuations. The arrangement includes a driver stage containing two current mirror circuits.

The invention is defined in claim 1 appended hereto. Preferred features are set out in the dependent claims.

As a result the invention allows a programmable logic output driver including a digital programming feature to maintain the output voltage slew rate at an acceptable value for either high or low values of load capacitances, the driver being operable so that it can maintain a constant value of the driver output resistance in the circumstances where the load voltage approaches the full swing logic voltage. Other aspects of the invention are exemplified by the attached claims.

In a preferred embodiment, the driver has a programmed output resistance that is independent of variations in process, temperature and VDD supply voltage. Such a driver can thus drive TTL loads with the minimum amount of required output current. Because of the constant resistance, the driver can be designed to supply a specified amount of current to a load even when the load is pulled down to a specified voltage. The resistance value is substantially the highest value possible consistent with providing a required minimum load drive current and the resistive damping of the output RLC circuit is maximized so that voltage "kicks" or "undershoot" is held to a minimum. According to this preferred embodiment, the output of a programmable bias generator is used to control the input gate of a switched current mirror (second bias current mirror), which provides a predetermined current gain. The output from the current mirror in turn controls the gate of an output drive device, but this gate can also be shunted to ground by a controllable switching device.

According to another aspect of the invention, a MOS device is included in one path to ground of the current mirror in order to compensate for the added resistance of a programmable switch included in the bias generator.

According to yet another aspect of the invention, a current generator that generates a small holding current which, under the control of a separate control signal, provides a holding current to the output drive device.

In yet another embodiment of the invention, multiple, controllable, switch mirrors (second bias current mirrors) and a mirror selection circuit are provided so that additional ranges for changing the conductance of the output stage are

incorporated.

It will thus be apparent that aspects of this invention can be implemented to provide an output driver that is programmable in order to maintain output voltage slew rates at an acceptable value for either high or low values of load capacitances. Moreover it is possible to provide an output driver which can be set so that the driver output resistance is substantially constant in the regime where the load voltage approaches the full swing logic voltage, whilst the programmed output resistance is independent of variations in process, temperature and VDD supply voltage.

Two significant benefits are derived from achieving constant output resistance, independent of process and supply voltage. The first is that in order to drive TTL (transistor-transistor-logic) loads properly, a specified amount of current must be supplied to the load when it is pulled down to a specified voltage. By considering the well known Ohms Law ("current equals voltage divided by resistance"), it is apparent that an output with constant resistance characteristics can always provide the specified minimum current at the specified minimum voltage because the ratio of a constant voltage to a constant current is a constant resistance. The second benefit is that by providing a constant driver output resistance, the resistor-inductor-capacitor (RLC) characteristics of the load are constant in the region where the output voltage nears the full swing logic voltage, especially logic 0. Because the resistance value is substantially constant and at the highest value possible consistent with providing a required minimum load drive current, the resistive damping of the output LC circuit is maximized and voltage "undershoot" or "kicks" are held to a minimum.

For a better understanding of the invention and to show how the same may be carried into effect, reference will now be made, by way of example, to the accompanying drawings, in which:

FIG. 1 is a schematic diagram illustrating a prior art bias generator;
FIG. 2 is a schematic diagram that shows generally certain principle features of one embodiment of the invention;
FIG. 3 is an embodiment of a programmable reference generator showing additional MOS devices used to compensate for the parasitic resistance of the MOS switches used in the programming;
FIG. 4a is a simplified schematic diagram illustrating the addition of power saving features to the programmable conductance output driver;
FIG. 4b is a timing diagram showing the relationship between input data and internal control signals;
FIG. 4c illustrates a control logic structure that can implement the required relationships shown in the timing diagram of FIG. 4b;
FIG. 5 is a schematic diagram showing MOS devices used for switches in a switched current mirror;
FIG. 6(a) is a schematic of a switch mirror block;
FIG. 6(b) is a symbolic representation of the switch mirror; and
FIG. 7 illustrates an embodiment of the invention providing the programming of four output conductance ranges.

A bias current generator according to the prior art is shown in FIG. 1. The gates of two P-channel devices P110, P120 are connected, as are the gates of two N-channel devices N110, N120. The sources of P110 and P120 are connected to a source of supply voltage and their drains are connected to the drains of the corresponding N-channel devices N110 and N120, respectively. The drains and gates of both P110 and N120 are connected. The source of N120 is connected to ground as is the source of N110, albeit over a resistor R150.

Assume that the N-channel devices N110 and N120 have the same effective width-to-length ratios W_e/L_e. Assume also that the P-channel devices P110 and P120 are constructed using m and n multiples of unit devices with the same W/L ratio. In such case, the total current through device P120 will be ml, the total current through device P110 will be nl and the ratio of current in P120 to P110 will therefore be m/n. With these conditions it can be shown using well known formulae that the operating conditions for the N-channel devices are given by:

$$\text{E1:} \qquad \text{Beta}\cdot W_e/L_e\cdot(V_o-V_t)=(2/R_{150})\cdot(\text{sqrt } m/n)\cdot(\text{sqrt } m/n - 1)$$

where Beta is the product of mobility and oxide capacitance, V_o is the NMOS gate voltage, V_t is the NMOS threshold, "sqrt" indicates the square root operator, and R_{150} is the value of the resistance of the resistor so labelled. Sometimes, the quantity (V_o-V_t) is expressed as the effective gate drive, that is, $V_o-V_t = V_e$. Making this substitution, the expression above becomes:

$$\text{E2:} \qquad \text{Beta } W_e/L_e\ (V_e) = (2/R_{150})\ (\text{sqrt } m/n)\ (\text{sqrt } m/n - 1)$$

This kind of bias circuit is commonly used in the prior art to establish a bias reference voltage for a constant current generator. The bias voltage V_e can then be found simply by re-arranging the terms in the last equation to yield:

E3: $V_e = [(2/R)\cdot(\text{sqrt } m/n)\cdot(\text{sqrt } m/n - 1)] / [\text{Beta}\cdot W_e/L_e]$

Unfortunately, the effective gate drive V_e is not constant over process or temperature in the bias generators of the prior art. Neither is the drain current constant, because the drain current Id for a MOS device in saturation is given by the known formula:

E4: $Id = \text{Beta } (W_e/L_e) (V_e)^2$

The embodiment of FIG. 2 improves upon the prior art generator shown in FIG. 1 by providing a programmable output conductance for a switchable output driver N320. As FIG. 2 shows, a modified bias generator is connected to a switched current mirror, which in turn is connected to a constant conductance output stage.

As FIG. 2 shows, the drain of N120 in the bias generator is connected to the gate of an N-channel device N210, whose source is grounded. A switch SW 160 and a resistor R151 are, furthermore, added in parallel to the bias generator between the resistor R150 and ground.

Supply voltage is connected to the sources of devices P210 and P220, which form either side of a conventional current mirror. The drain of P210, however, is connected to the drain of the N-channel device N210, which controls the voltage at the gates of current mirror devices P210 and P220, as well as at the drain of P210. As is common in current mirrors, the gate and drain of the device P210 are connected to the gate of the following P-channel device P220, whose source is connected to the supply voltage and whose drain is connected as described below to a constant conductance output stage.

The operation and implementation of current mirrors are well understood by designers of digital integrated circuits and are therefore not described in further detail here. Of note, however, is that the current of device P210 is cI, while the current of device P220 is dI. The increase, or gain, in current is therefore equal to dI/cI = d/c.

As FIG. 2 shows, the source of P220 is connected to a constant conductance output stage, more particularly to the gate and drain of an N-channel device N310, to the gate of an N-channel output drive device N320 and to ground via a switch SW470B. The gate and drain of N310 are connected, and the source of N310 is grounded. The gates of N310 and N320 are connected.

The drain of the output drive device N320 is connected to the output line of the circuit, which will normally be tied to the TTL device the system is to drive. The source of N320 is grounded.

Because the programmable bias generator is coupled to the output driver through a current mirror, with current gain that is independent of process, temperature and voltage, the output driver N320 provides a programmable drive logic signal that has several desirable properties that are also independent of process, temperature, and voltage.

The independence of the output conductance of the output driver N320 from process, temperature and voltage may be seen from the commonly used equation for output conductance $g_{o[320]}$:

E5: $g_{o[320]} = \text{Beta}\cdot(W_e[320]/L_e[320])\cdot(V_e[320])$

Note that if the devices N310 and N210 are made equal in size, the effective gate drive of N310 and output device N320 may be increased in accordance with the current gain d/c of the switched mirror. The mirror current gain is fixed at d/c since the P-channel devices P210 and P220 are preferably constructed using c and d multiples of unit devices with the same width-to-length ratio W/L.

Using known formulae one can show that the effective gate drive $V_{e[320]}$ of N320 is related to the effective gate drive V_e of the programmable bias generator simply by the square root of the mirror current gain d/c, thus:

E6: $V_{e[320]} = V_e \text{ sqrt}(d/c)$

A combination of expressions E2 and E4-E6 above then yields the following:

E7: $g_{o[320]}=\text{sqrt}(d/c)\cdot[2/(R_{150})]\cdot(\text{sqrt } m/n)\cdot(\text{sqrt } m/n-1)$

In the bias generator, switch SW 160 provides a resistance value of R150 between the source of N110 and ground when it is closed, since resistor R151 will be shunted. When switch SW 160 is opened, however, the resistance value will be $R_{150} + R_{151}$ (since source current will then have to pass through both resistors) and the driver output conductance

will be decreased, as can be seen from the following expression, in which the denominator of the second term in the right-hand side is increased from R_{150} to $(R_{150}+R_{151})$:

$$E8: \quad g_{o[320]}=\text{sqrt}(d/c)\cdot[2/(R_{150}+R_{151})]\cdot(\text{sqrt } m/n)\cdot(\text{sqrt } m/n-1)$$

As is mentioned above, this decrease is desirable when driving low-capacitance loads.

Switch SW 470B is used to turn on the output current when it is in the open condition as shown. For a positive logic output, the open condition would correspond to a logic "0", or a LOW voltage output. For a logic "1" output, SW 470B would be closed, whereby the gate voltage on N320 would drop to a value sufficiently low to turn N320 off.

The delay time to turn on the output drive device N320 tends to be constant since the current driving the gate of N320 tends to track the same variations in process, voltage, and temperature as does the variation of V_e. For example, as V_e increases with temperature to require that a higher turn-on voltage be reached, the input current to the output device will increase in the same proportion because it is derived from a constant conductance generator.

Noting now that $\text{Beta}\cdot(W_e/L_e)\cdot V_e^2$ may be re-written as $V_e\cdot[\text{Beta}\cdot(W_e/L_e)\cdot V_e]$, one may then combine expressions E4 and E5 (taking the general version of E5 rather than the specific equation for $g_{o[320]}$) to yield:

$$E9: \quad I = V_e\cdot G$$

The delay time T required for the input voltage to traverse the span V_e is therefore:

$$E10: \quad T = V_e\cdot(C_{input}/I) = C/G$$

Where the input capacitance is determined largely by the gate capacitance of the output device, which typically varies less than 5 percent, the variation in T will therefore be small since G is independent of process and temperature.

The programming switch SW 160 shown in FIG. 2 may alternatively be provided with a bond wire jumper, or preferably a MOS switch. Such an arrangement is shown in FIG. 3. With reference to FIG. 3, as the bias generator is provided with a MOS switch, then a MOS device such as N160 is added to the generator to compensate for the added resistance of either switch N170 or N180. Where N170 or N180 are equal in size, and the ratio of current between the devices P110 and P120 is m/n (as is indicated in FIG. 3), the appropriate sizing for N160 is just sqrt(m/n) times the size of switch N170 or N180. This sizing assures the same voltage drop across N160 as across N170 or N180.

Also with reference to FIG. 3, where the bias generator drives the input stage of a current mirror which produces an output current cI, then an additional device N280, with a width-to-length ratio W/L of c/sqrt(mn) is added to the mirror to compensate for the switch effects. This W/L value assures that the voltage drop across N280 will be equal to the voltage drop across N160.

The advantage provided by the compensating MOS devices N170, N180 and N280 of FIG. 3 is that they greatly reduce the temperature-dependent and process-dependent effects of the switches N170 and N180 in causing variations in the programmed value of output conductance. The primary variations in output conductance will then depend only on the temperature coefficient and accuracies of resistors chosen for R150 and R151. These resistors may be polysilicon resistors, well resistors, or deposited film resistors, depending on available processes, specific resistance value, and the required temperature coefficient.

FIGS. 4a-4c illustrate two improvements to the embodiment of the invention shown in FIG. 2. Both improvements result in reduced standby power for the output driver.

The switched current mirror of FIG. 2 passes current continuously, even when the circuit is not required to provide an output current as is the case when S470B is closed. The improvement in FIG. 4a is the addition of switches SW260A and 260B, which interrupt the flow of current from device N210 to P220 and short out the gate of P210 to the positive supply voltage. Both of these actions cause the current flow cI and dI to be reduced to zero after the high-current initial phase of driving a capacitive load is no longer required.

Once the current from P220 has been forced to zero, some minimum value of output current drive must be provided by output device N320. This minimum value of output current is provided by a small holding current generator (labelled "i gen" in FIG. 4a), which passes current hI through switch SW 470A and across device N420. Even this small holding current hI is not required for a data output of logic "1" when SW 470B is closed and no current flows through output device N320. Consequently, the holding switch SW 470A is closed when the "N ON" is HIGH, whereas the switch SW 470B at the gates of N310 and N320 is in the open position for the "N ON" portion of the timing cycle.

A load capacitance charging signal CHG controls the state of a switch between the supply voltage and the gates

of the devices P210 and P220 in the current mirror. This charging signal CHG need be present for only as long as required to assure that the load capacitance has rapidly reached the full logic output voltage. The CHG signal may be generated for the required amount of time by any conventional logic circuitry that detects transition of input data from the logic "0" to the logic "1" value.

FIG. 4b illustrates the timing relationship between the signals N ON, its inverse N OFF, the charge signal CHG and the state of an input data bit DATA IN. An example of suitable detection circuitry that has these timing characteristics is illustrated in FIG. 4c, but other circuits may also be used together with the invention. Theory and experience indicate that the CHG signal will be required for less than 100 nanoseconds in typical applications.

The signals CHG, N ON and N OFF may be generated in a circuit indicated generally as circuit 600 in FIG. 4c. Referring to this figure, when the input data (DATA IN signal) transitions from a "1" to a "0" as shown in FIG. 4a, an MOS capacitor N620 will no longer be clamped to ground, but rather will begin to charge through a switch P630. The switch P630 receives a constant current from the constant current generator consisting of the 16k resistor (for example) and the mirror P610, P620.

Immediately when the DATA IN signal changes from a "1" to a "0", N ON changes from a "0" to a "1" and the convention NAND gate output changes from a "1" to a "0". The output from the NAND gate passes through an inverter an becomes the CHG signal, which changes from a "0" to a "1". This CHG signal is then routed to the switch mirror, whereas the N ON signal is used to turn on the small holding current generator.

As the MOS capacitor N620 charges past the logic threshold of the inverter connected to its top plate, (its gate), the inverter output changes from "1" to "0" and causes the NAND gate output to rise from "0" to "1", thereby driving the CHG signal from "1" to "0". The size of the MOS capacitor may be chosen for any desired duration of the CHG signal, for example, from 10 to 100 nanoseconds.

When the DATA IN signal changes from "0" to "1", the CHG signal is immediately terminated and the MOS capacitor discharges rapidly through the N-channel device N610. At the same time, the N ON signal changes from "1" to "0" and immediately turns off the small holding current generator. The N OFF signal (the inverse of N ON) also changes from "0" to "1", turns on the switch SW 470A, and immediately turns off the output driver N320 by shorting its gate to ground. The switch and charging control signals N ON, N OFF, CHG, and those applied to the various switches in the embodiments of the invention may alternatively be generated in a known manner by other conventional hardware structures.

FIG. 5 is a schematic diagram showing the MOS devices preferably used to implement the various switches in the system that are controlled by the CHG signal. Thus, the P-channel MOS device P260B corresponds to the switch SW 260B in FIG. 4a; switch SW 260A is implemented by P260A; and switch SW 360 is implemented by the N-channel device N360. Also, switch SW 470 B, which is controlled by the N OFF signal, is shown implemented by the N-channel device N470B. The implementation of simple switches such as these is well understood in the field of circuit design.

In FIG. 6a and 6b, the switched mirror and its symbolic block representation are shown. In this block representation, the switched mirror receives the input signal INPUT as before from the drain of the device N120 of the bias generator (see FIG. 5). An ON signal is also applied to the mirror; this ON signal corresponds to the CHG signal shown and described above. As FIG. 6b indicates, the current mirror acts to provide an output current that is d/c times its input current; this is also described above.

A switched current mirror using a lower current ratio than the ones used for the charging current may be used to provide the small holding current generator indicated in FIG. 5. Such an arrangement is shown in FIG. 7.

In the embodiments described above, a single switched current mirror stage with a current gain of d/c is included between the bias generator and the constant capacitance output stage. The system according to the invention is not limited to such single-value implementations.

FIG. 7 illustrates an embodiment of the invention which provides four charging current ranges for programming. Two switched mirrors are included to provide two programmable levels of output current from the generator at output devices N320A or N320B. The two switched mirrors preferably have the same structure as described above for the single-mirror implementations and are indicated generally at 510 and 550 in FIG. 7.

Note that the output stage in this embodiment includes a pair of output devices N320A and N320B, each corresponding to the single driver N320 in FIG. 5, as well as a set of gate control devices corresponding to N310, N360 and each with a switch N370A, N370B corresponding to the single switch N470B in FIG. 5. The drains of the two output drive devices N320A and N320B are connected. The gates of the devices N360A and N360B are connected to the CHG signal. The drains and gates of devices N310A and N310B are connected, respectively, to the outputs of the switch mirrors 510 and 550 (controlled by the CHG signal) and 410 and 450 (controlled by the N ON signal. These current mirrors preferably have the structure shown in FIGS. 6a and 6b.

According to this embodiment, switch mirror 550 is enabled only if the "RANGE C" programming control circuit is a logic "0". In that case, a P-channel device P660 in a RANGE C Switch 700 (which forms a mirror selection switching device) is driven into a conductive state and the bias generator output voltage at the drain of N120 is allowed to pass to the input of switch mirror 550.

In the case that the switch mirror located at 550 is to be disabled by a logic "1" for the RANGE C control signal,

P660 is cut off and N660 is turned on and grounds the input of switch mirror 550. In addition, device N670 is turned on to return any leakage current from mirror 550 output to ground and to assure that the output driver N320B is turned off.

Holding current mirrors 410 and 450 provide a small holding current to guarantee that the N320A and N320B outputs remain on at a desired output conductance value after the initial charging phase is complete. By using switch mirror blocks as shown in FIGS. 6a and 6b, which are connected to the input bias generator, the driver output conductance level is constant and independent of process, temperature and power supply variation.

Holding current mirrors 410 and 450 must be turned off to save power when the data input is a logic "1". This is accomplished by using the signal N ON to drive an ON input to each switch mirror 410, 450. The N ON signal is derived from an inverter connected to the logic input, and is thus the logical inverse of the input data bit. Switch devices N370A and N370B short all switch mirror leakage current to ground in response to the N OFF signal (the logical inverse of N ON) when the data input is a logic "1". These switches assure that output devices N320A and N320B are turned off. The N OFF signal is derived from a logic buffer consisting of two inverters connected is series and to the data input (see FIG. 4c).

By varying device sizes and current gains in the switched mirrors 510 and 550 and also by varying the sizes of the output devices N320A and N320B, many possible programming ranges may be provided. The highest output conductance in the preferred embodiment is programmed by setting RANGE A (at the input of the bias generator) equal to logic "1" and RANGE C equal to a logic "0". Although four programming ranges may be selected by the combination of the RANGE A and RANGE C logic signals in the embodiment of FIG. 7a, many more programming ranges are possible by using additional programming resistors or switched mirrors. In other words, more than two complete switch mirrors 510/410 and 550/450 may be included, as long as additional selection switches are included in the RANGE C switching device and suitable control signals are provided as above.

Additionally, the invention is not restricted by the polarity of the embodiments illustrated in the figures. The invention may be easily extended using known methods to add switched mirrors and output drivers of opposite polarity to drive CMOS loads, or use alternate semiconductor technology to drive loads of different output voltages or signal polarities.

Claims

1. A logic output driver, for driving an attached logic device, including a bias generator (100) that has a first bias current mirror (P110,P120) and a pair of bias output devices (N110,N120), the driver further including a second bias current mirror (200; P210, P220) connected to the bias generator (100), an output stage (300) connected to the second bias current mirror (200), and at least one of the group consisting of the bias generator (100), the output stage (300) and the second bias current mirror (200) having a switch (160,700, SW360) wherein:

   the second bias current mirror (200) has a mirror input gate (N210) connected to one of said pair of bias output devices of the bias generator; and
   the output conductance of the output stage (300) is dependent on the state of said switch;
   whereby said switch can be programmably operated to select one of a predetermined number of predetermined substantially constant output conductances of the output stage (300) while a load voltage (320) varies; and
   wherein a pair of bias resistors (R150, R151) is included in the path to ground of a predetermined one of said pair of bias output devices of the bias generator (100) and a first bias programming switching device is included in the path to ground of the same bias output device as the bias resistors (R150, R151).

2. A logic output driver according to claim 1 in which a second bias programming switching device is included in the path to ground of the same bias output device as the bias resistors.

3. A logic output driver according to claim 2, in which a resistance compensation device (N160) is included in the path to ground of the other of said pair of output devices of the bias generator (100) to compensate for the resistance of the bias programming switching devices (N170, N180).

4. A logic output driver according to claim 1, wherein the switch (160) selects a bias voltage (V_e) of the bias generator (100).

5. A logic output driver according to claim 1, wherein the switch (360) selects a conductance of the output stage (300).

6. A logic output driver according to any one of the preceding claims wherein the output stage (300) includes an output drive device (N320) and there is a two-state output semiconductor switch (SW 470B) to conduct and shunt a gate of the output drive device (N320) when an input data bit has a first state and to open when the input data

bit has a second state.

7. A logic output driver according to any one of the preceding claims and comprising a switchable current holding circuit, comprising a holding current generator (i_gen) and a holding switch SW 470A), included in the output stage to maintain a minimum output current at a predetermined slew rate into the load when the load is in a low logical state.

8. A logic output driver according to any one of the preceding claims, wherein the second bias current mirror (200) includes a quick-charging arrangement (600) that generates a charging signal (CHG) as a predetermined function of state transitions of the load.

9. A logic output driver according to any one of the preceding claims and including a plurality of said second bias current mirrors (510, 410; 550, 450), each having a different output current, and a mirror selection device (700) connected to the bias generator (100) and to the second bias current mirrors that is activated by a selected input signal (RANGE_C).

Patentansprüche

1. Logikausgangstreiber zum Ansteuern einer angebrachten Logikvorrichtung, der einen Vorspannungsgenerator (100) beinhaltet, der einen ersten Vorspannungsstromspiegel (P110, P120) und ein Paar von Vorspannungsausgabevorrichtungen (N110, N120) beinhaltet, wobei der Treiber weiterhin einen zweiten Vorspannungsstromspiegel (200; P210, P220), der mit dem Vorspannungsgenerator (100) verbunden ist, und eine Ausgangsstufe (300) beinhaltet, die mit dem zweiten Vorspannungsstromspiegel (200) verbunden ist, und mindestens eines der Gruppe, die aus dem Vorspannungsgenerator (100), der Ausgangsstufe (300) und dem zweiten Vorspannungsstromspiegel (200) besteht, einen Schalter (160, 700, SW360) aufweist, wobei:

   der zweite Vorspannungsstromspiegel (200) ein Spiegeleingangsgatter (N210) aufweist, das mit einem Ende des Paares von Vorspannungsausgabevorrichtungen des Vorspannungsgenerators verbunden ist; und

   der Ausgangswirkleitwert der Ausgangsstufe (300) von dem Zustand des Schalters abhängig ist;

   wodurch der Schalter programmierbar betätigt werden kann, um einen einer vorbestimmten Anzahl von vorbestimmten im wesentlichen konstanten Ausgangswirkleitwerten der Ausgangsstufe (300) auszuwählen, während sich eine Lastspannung ändert; und

   wobei ein Paar von Vorspannungswiderständen (R150, R151) in dem Pfad zu Masse einer vorbestimmten des Paares von Vorspannungsausgabevorrichtungen des Vorspannungsgenerators (100) beinhaltet ist, und eine erste Vorspannungsprogrammierungsschaltvorrichtung in dem Pfad zu Masse der gleichen Vorspannungsausgabevorrichtung wie die Vorspannungswiderstände (R150, R151) beinhaltet ist.

2. Logikausgangstreiber nach Anspruch 1, bei welchem eine zweite Vorspannungsprogrammierungsschaltvorrichtung in dem Pfad zu Masse der gleichen Vorspannungsausgabevorrichtung wie die Vorspannungswiderstände beinhaltet ist.

3. Logikausgangstreiber nach Anspruch 2, bei welchem eine Widerstandkompensationsvorrichtung (N160) in dem Pfad zu Masse der anderen des Paares von Ausgabevorrichtungen des Vorspannungsgenerators (100) beinhaltet ist, um den Widerstand der Vorspannungsprogrammierungsschaltvorrichtungen (N170, N180) zu kompensieren.

4. Logikausgangstreiber nach Anspruch 1, bei dem der Schalter (160) einer Vorspannung (V_e) des Vorspannungsgenerators (100) auswählt.

5. Logikausgangstreiber nach Anspruch 1, bei dem der Schalter (360) einen Wirkleitwert der Ausgangsstufe (300) auswählt.

6. Logikausgangstreiber nach einem der vorhergehenden Ansprüche, bei dem die Ausgangsstufe (300) eine Ausgangsansteuerstufe (N320) beinhaltet und es einen Ausgangshalbleiterschalter (SW470B) mit zwei Zuständen gibt, um ein Gate der Ausgangsansteuerstufe (N320) durchzuschalten und nebenzuschließen, wenn ein Eingangs-

datenbit einen ersten Zustand aufweist, und zu öffnen, wenn das Eingangsdatenbit einen zweiten Zustand aufweist.

7. Logikausgangstreiber nach einem der vorhergehenden Ansprüche, der eine schaltbare Stromhalteschaltung aufweist, die einen Haltestromgenerator (i_gen) und einen Halteschalter (SW470A) aufweist, die in der Ausgangsstufe beinhaltet sind, um einen minimalen Ausgangsstrom bei einer vorbestimmten Anstiegsgeschwindigkeit in der Last aufrechtzuerhalten, wenn sich die Last in einem logisch niedrigen Zustand befindet.

8. Logikausgangstreiber nach einem der vorhergehenden Ansprüche, bei dem der zweite Vorspannungsstromspiegel (200) eine Schnelladeanordnung (600) beinhaltet, die ein Ladesignal (CHG) als eine vorbestimmte Funktion von Zustandsübergängen der Last erzeugt.

9. Logikausgangstreiber nach einem der vorhergehenden Ansprüche, der eine Mehrzahl von zweiten Vorspannungsstromspiegeln (510, 410; 550, 450), von denen jeder einen unterschiedlichen Ausgangsstrom aufweist, und eine Spiegelauswahlvorrichtung (700) beinhaltet, die mit dem Vorspannungsgenerator (100) und mit den zweiten Vorspannungsstromspiegeln verbunden ist, die durch ein ausgewähltes Eingangssignal (RANGE_C) ausgewählt wird.

Revendications

1. Circuit de commande de sortie logique pour commander un dispositif logique associé, comportant un générateur de polarisation (100) doté d'un premier miroir de courant de polarisation (P110, P120) et d'une paire de dispositifs de sortie de polarisation (N110, N120), le circuit de commande comportant en outre un second miroir de courant de polarisation (200 ; P210, P220) relié au générateur de polarisation (100), un étage de sortie (300) relié au second miroir de courant de polarisation (200), l'un au moins des éléments du groupe constitué par le générateur de polarisation (100), l'étage de sortie (300) et le second miroir de courant de polarisation (200) étant doté d'un interrupteur (160, 700, SW360) caractérisé en ce que :

   le second miroir de courant de polarisation (200) comporte une porte d'entrée miroir (N210) reliée à l'un des dispositifs de ladite paire de dispositifs de sortie de polarisation du générateur de polarisation ; et

   la conductance de sortie de l'étage de sortie (300) est fonction de l'état dudit interrupteur ;

   ledit interrupteur peut être commuté par programme pour effectuer la sélection d'une conductance parmi un nombre prédéfini de conductances essentiellement constantes définies au préalable de l'étage de sortie (300), selon les variations d'une tension de charge (320) ; et

   une paire de résistances de polarisation (R150, R151) est placée dans le circuit de mise à la terre d'un dispositif déterminé au préalable de ladite paire de dispositifs de sortie de polarisation du générateur de polarisation (100) ; et un premier dispositif de commutation de polarisation programmable est placé dans le circuit de mise à la terre du même dispositif de sortie de polarisation que pour les résistances de polarisation (R150, R151).

2. Circuit de commande de sortie logique selon la revendication 1, dans lequel un second dispositif de commutation de polarisation programmable est placé dans le circuit de mise à la terre du même dispositif de sortie de polarisation que pour les résistances de polarisation.

3. Circuit de commande de sortie logique selon la revendication 2, dans lequel un dispositif de compensation de résistance (N160) est placé dans le circuit de mise à la terre de l'autre dispositif de ladite paire de dispositifs de sortie du générateur de polarisation (100) pour compenser la résistance du dispositif de commutation de polarisation programmable (N170, N180).

4. Circuit de commande de sortie logique selon la revendication 1, dans lequel l'interrupteur (160) permet la sélection d'une tension de polarisation (V_e) du générateur de polarisation (100).

5. Circuit de commande de sortie logique selon la revendication 1, dans lequel l'interrupteur (360) permet la sélection d'une conductance de l'étage de sortie (300).

6. Circuit de commande de sortie logique selon l'une quelconque des revendications précédentes, dans lequel l'étage

de sortie (300) comprend un dispositif de commande de sortie (N320), et dans lequel un interrupteur statique de sortie à deux états (SW 470B) est fermé et court-circuite la porte du dispositif de commande de sortie (N320) lorsqu'un bit de données d'entrée est à un premier niveau, et ouvert lorsque le bit de données d'entrée est à un second niveau.

7. Circuit de commande de sortie logique selon l'une quelconque des revendications précédentes, comprenant en outre un circuit de maintien de courant commutable, comprenant un générateur de courant de maintien (i_gen) et un interrupteur de maintien SW 470A, inclus à l'étage de sortie pour maintenir dans la charge un courant de sortie minimal avec une vitesse de saut prédéterminée, lorsque la charge est au niveau logique bas.

8. Circuit de commande de sortie logique selon l'une quelconque des revendications précédentes, dans lequel le second miroir de courant de polarisation (200) comporte un système de charge rapide (600) qui génère un signal de charge (CHG) en tant que fonction définie au préalable des changements d'état de la charge.

9. Circuit de commande de sortie logique selon l'une quelconque des revendications précédentes, comprenant en outre plusieurs desdits seconds miroirs de courant de polarisation (510, 410 ; 550, 450) susdits, chacun d'eux ayant un courant de sortie différent, ainsi qu'un dispositif de sélection de miroir (700), relié au générateur de polarisation (100) et aux seconds miroirs de courant de polarisation, qui est activé par un signal de sélection d'entrée (RANGE_C).

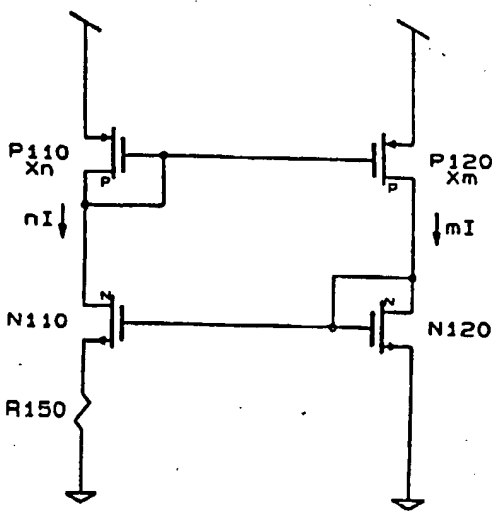

Figure 1
Bias Generator
(Prior Art)

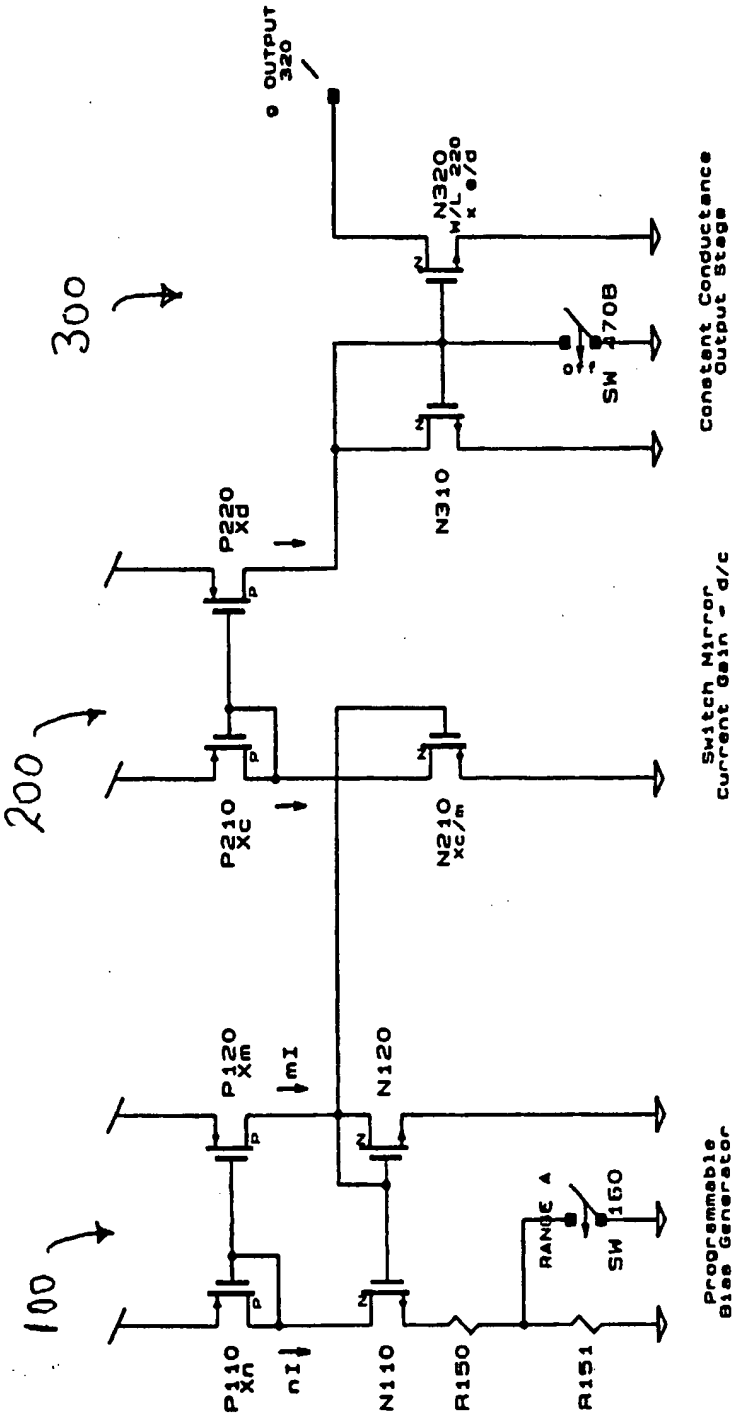

Figure 2
Programmable Conductance
Output Driver

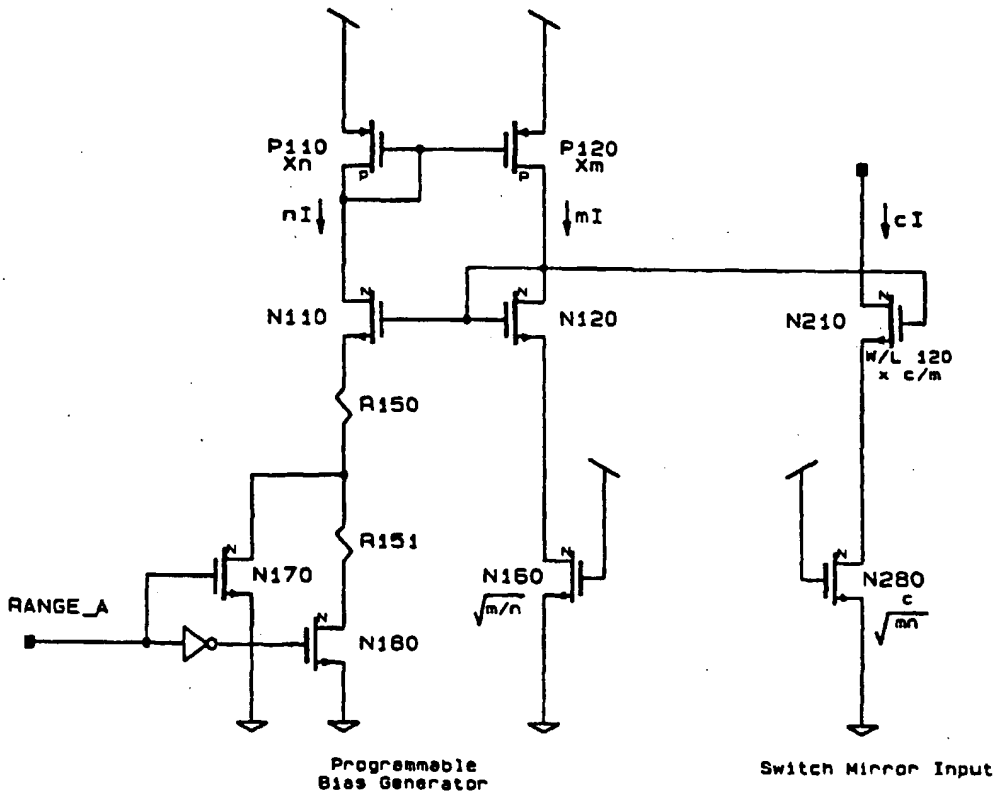

Figure 3
Programmable Reference Generator
With MOS Switching

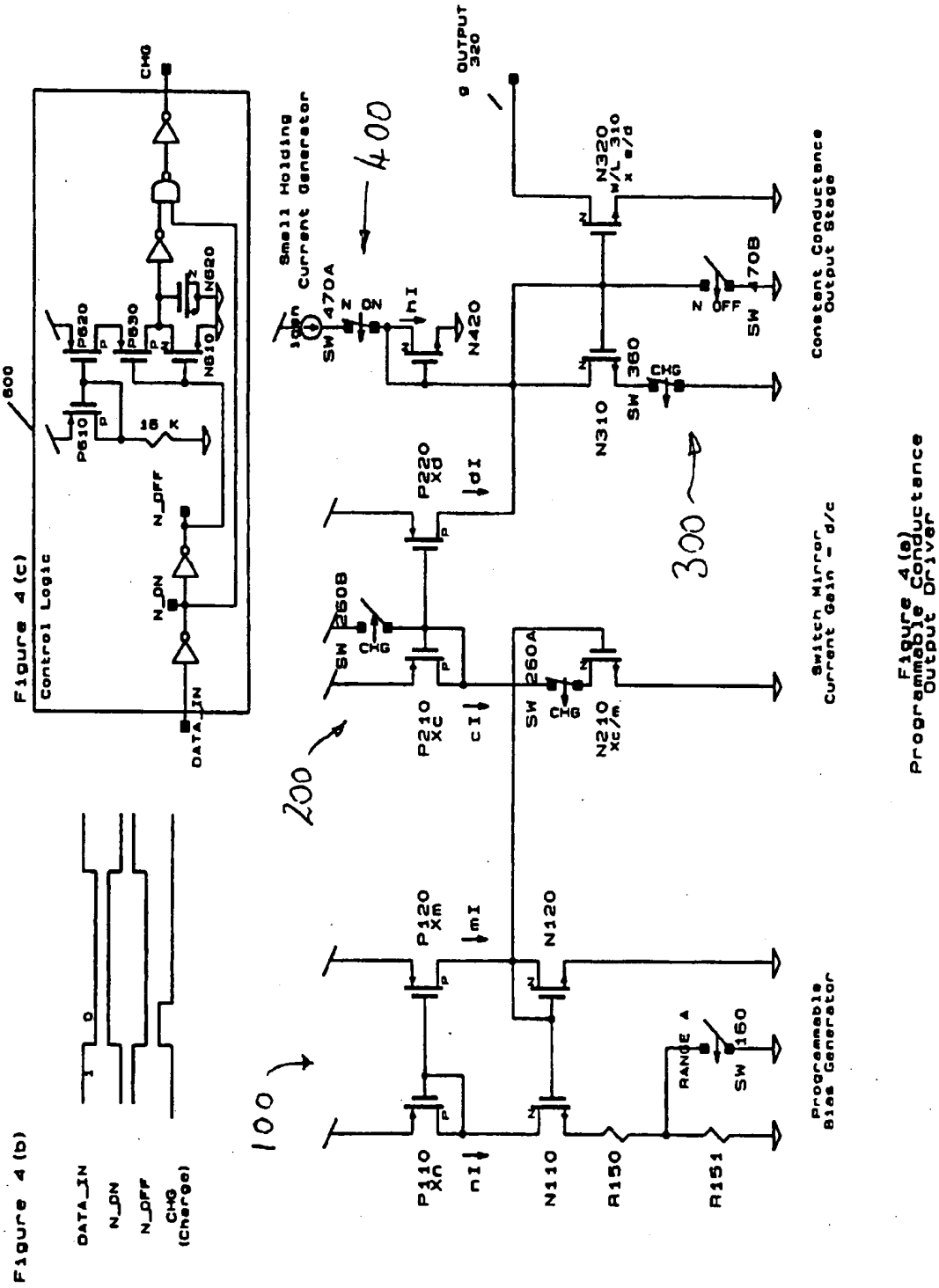

Figure 4 (a)

Figure 4 (b)

Figure 4 (c)

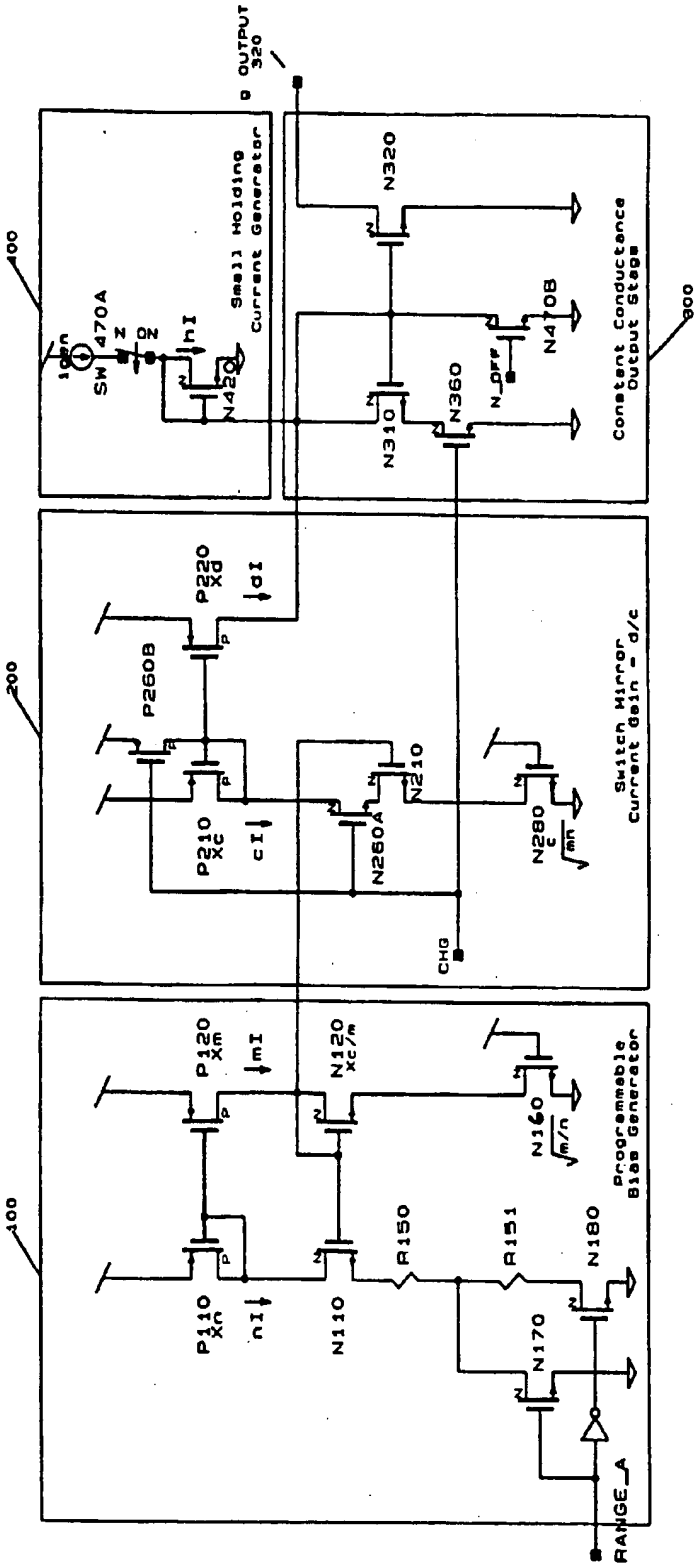

Figure 5
Programmable Conductance
Output Driver
With MOS Transistor Switching

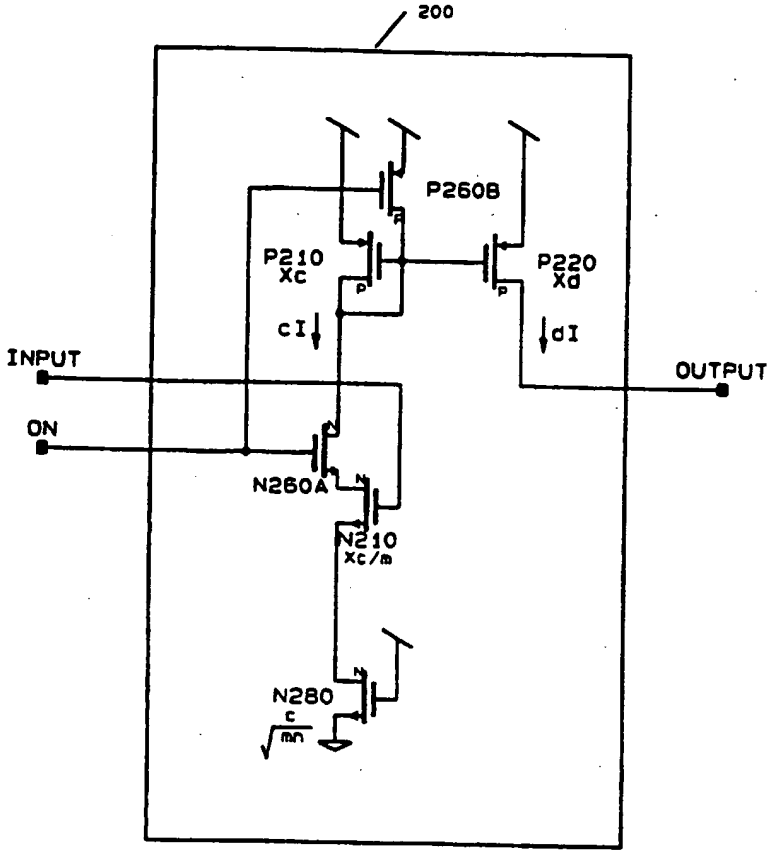

Figure 6(a)
Switch Mirror
Current Gain = d/c

Figure 6(b)
Switch Mirror
Block Symbol
Current Gain = d/c

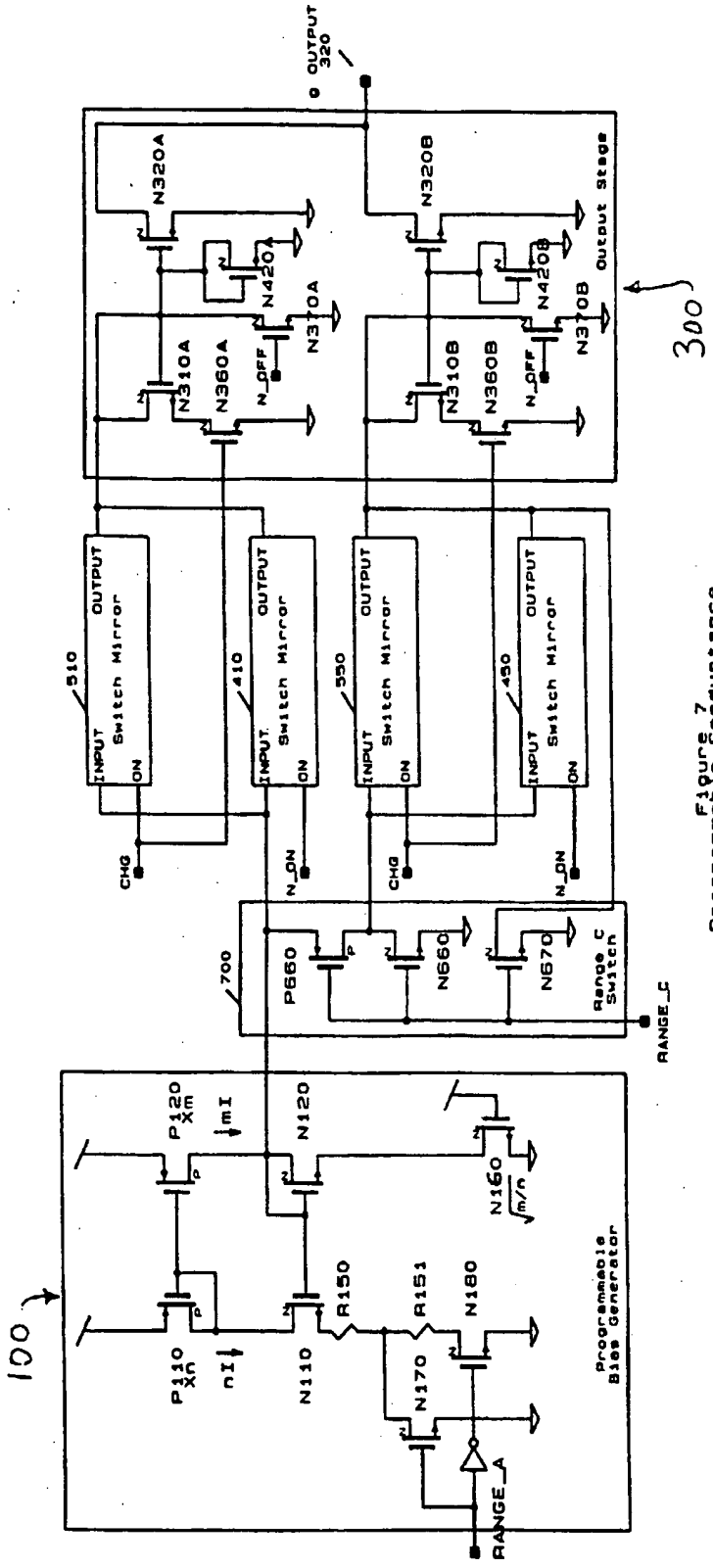

Figure 7
Programmable Conductance
Output Driver

INTERNATIONAL SEARCH REPORT

International Application No
PCT/IB 03/05166

A. CLASSIFICATION OF SUBJECT MATTER
IPC 7 H03K19/003 H03K17/16

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
IPC 7 H03K

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practical, search terms used)
EPO-Internal, WPI Data, PAJ, IBM-TDB

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category °	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	US 6 281 730 B1 (VU HA CHU) 28 August 2001 (2001-08-28)	1,12-15
A	column 3, line 39 - column 7, line 67; figures 1-3	3,4,10, 11
X	EP 0 575 676 A (PIONEER DIGITAL DESIGN CENTRE) 29 December 1993 (1993-12-29)	1,17
A	column 8, line 7 - column 9, line 41; figures 4a-4c	3,6
X	US 4 825 099 A (BARTON STEVEN K) 25 April 1989 (1989-04-25)	1
A	column 2, line 61 - column 4, line 68; figures 1,2	3
A	US 5 021 730 A (SMITH MICHAEL D) 4 June 1991 (1991-06-04) column 3, line 27 - line 59; figure 1	1,2

-/--

[X] Further documents are listed in the continuation of box C.

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Date of the actual completion of the international search	Date of mailing of the international search report
24 August 2004	02/09/2004

Name and mailing address of the ISA	Authorized officer
European Patent Office, P.B. 5818 Patentlaan 2 NL – 2280 HV Rijswijk Tel. (+31-70) 340-2040, Tx. 31 651 epo nl, Fax: (+31-70) 340-3016	Feuer, F

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INTERNATIONAL SEARCH REPORT

International Application No
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C.(Continuation) DOCUMENTS CONSIDERED TO BE RELEVANT

Category °	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
A	PATENT ABSTRACTS OF JAPAN vol. 1995, no. 09, 31 October 1995 (1995-10-31) & JP 07 146726 A (OKI ELECTRIC IND CO LTD), 6 June 1995 (1995-06-06) abstract -----	1,2

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